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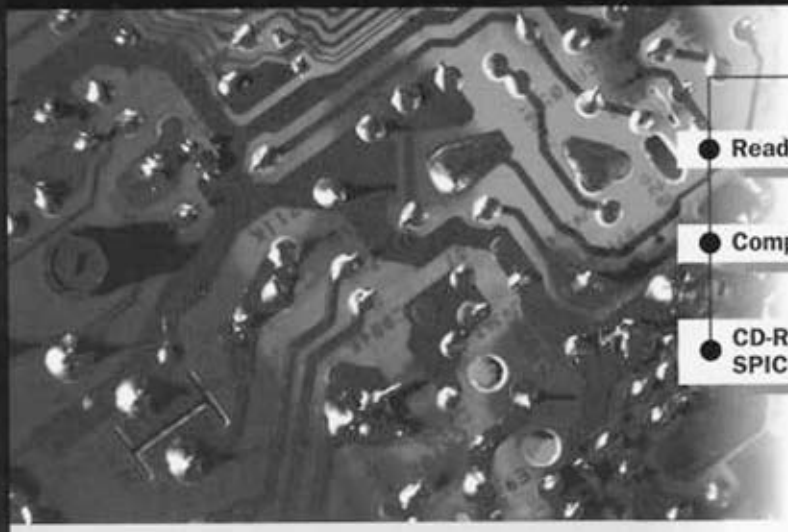

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Switch-Mode Power Supply SPICE Cookbook

Christophe P. Basso

SWITCH-MODE POWER SUPPLY SPICE COOKBOOK

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Christophe P. Basso

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To Lucille, Paul, and my wife, Anne.

CONTENTS

FOREWORD

In the mid-1960s, it was popular to say that switch-mode power supplies were always one microsecond away from disaster. And there was plenty of evidence to support this seemingly cynical comment. Even the manufacturers themselves did not understand completely the various failure mechanisms of their new bipolar power transistors. Users were contributing to the problem by doing things like connecting these devices in parallel for increased power-handling capability, and using "seat of the pants" frequency compensation techniques for stability. Designs that seemed to work in the lab failed in the field. On the other hand, if the design worked well in the field, the designers often had no idea why it did. In fact, they may not have been so-called power supply designers at all, but rather general-purpose engineers who had to design their own power supplies as a "necessary evil" along with their other "more important" modules. Or they may have been young engineers who were handed power supply designs as learning experiences because their bosses thought this would be simple. Therefore, despite the apparent size, weight, and efficiency advantages of switch-mode power supplies, it took many years for them to become generally accepted.

By contrast, today we take the high reliability of switch-mode power supplies for granted. Materials are better. Devices are better and are better understood. Integrated circuit controllers, well supported by excellent application notes, are now available. The fact that power supply reliability depends upon good manufacturing processes and good mechanical/thermal design, as well as good electrical design, is better recognized. Furthermore, power supply design, as part of the more inclusive field of power electronics, has become recognized as a *bona-fide* branch of electrical engineering. A young power supply designer today is likely to be a member of a well-managed, centralized power supply design-engineering staff, and is likely to have taken power electronics classes while in school.

Another key ingredient in reliable power supply design is reliable, easy-to-use simulation models. The early SPICE models that were geared for the burgeoning microelectronics revolution, and that may be appropriate for analyzing switching behavior over a single cycle, are not as appropriate for analyzing power supply step-load response or stability margin, for example. Today, the integrity of these switch-mode power supply simulation models is high enough that even engineers who are non-experts in detailed power supply behavior per se can design reliable switch-mode power supplies. This last point will become increasingly

important as the next-generation microelectronic supply voltages become lower and lower, dictating an increasingly distributed power conversion architecture, to the point where in many cases it will be difficult to tell exactly where the power supply leaves off and the user electronics begin.

In this book, Christophe Basso takes a unique, refreshing, all-inclusive approach to switch-mode power supply modeling, with emphasis on SPICE-derived models because of their ease of use. As an application engineer by profession, he consistently takes the user's point of view, providing the information necessary to understand basic concepts while leaving the details to the references. After tracing the historical development of these models, he provides comparisons that highlight their relative strengths and weaknesses. Christophe Basso then models some of the most common switch-mode power supply topologies, including the BUCK, BOOST, BUCK-BOOST, and SEPIC, which is enjoying a revival of sorts because of its applicability to distributed power supplies. Enough detail is provided to enable the user to apply these models to topologies not included in the book as well.

The specific chapter titles are:

- Overview
- Generic Models for Faster Simulations
- Topology-by-Topology Simulation Recipes
- More Complex Simulations
- Self-Oscillating Power Supplies

In addition, there are four appendixes:

- Applying the K Factor for Quick Pole-Zero Compensation
- Feeding the Transformers Models with Physical Values
- Conducted EMI Filter Design
- CD-ROM Content

A CD-ROM is included with the book, and a Web site is planned, which will enable the user to download additional models on a continuing basis, and to feed back questions, comments, and lessons learned. *Switch-Mode Power Supply SPICE Cookbook* represents a welcome, easy-to-read, results-oriented addition to the power supply design literature.

DANIEL M. MITCHELL
DM MITCHELL CONSULTANTS
CEDAR RAPIDS, IOWA, USA

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CHAPTER 1

Overview

User friendliness is a key factor for the commercial success of any simulation program. The growing complexity of integrated circuits and equipment make this aspect more and more important. Despite numerous publications devoted to the *Simulation Program with Integrated Circuit Emphasis* (SPICE), it still frightens the novice when its name is pronounced.

Developed in the mid-1970s by the University of California, Berkeley, the primary aim of the SPICE program was to fulfill the needs of the electronics industry—mainly integrated circuit makers. However, with the support and funds from private editors, the SPICE program has evolved over a number of years into many practical and affordable packages, with emphasis on providing both low-priced and friendly access to beginners.

The performance of SPICE can significantly help you speed up the design phase of the equipment you are currently working on, even if SPICE is not able to generate an electronic schematic by itself! Thus, the faster the IC is designed, the quicker it will be operational on the market and, of course, the bigger the smile will be that appears on your boss's face. Moreover, SPICE is inherently efficient because if you start working with an unfamiliar concept, it will enable you to quickly grasp the full meaning of any particular architecture.

For instance, what would happen if you, the company's analog or microprocessor expert, were suddenly told to replace the universal 2.2μF in series with the mains by a *Switch-Mode Power Supply* (SMPS) because it is cheaper and more reliable? This results in you not having time to spare in "guide" books that will only give you headaches instead of helping you. This book has been written so newcomers to the power electronics world can overcome any SMPS design questions.

"Do You Really Need to Simulate?"

How many times have you heard this query when asking for a simulation package or a new computer? The following statements do not represent an exhaustive list of pros about computer simulation, but they can certainly be thought of as a "help list" available during the negotiations.

1. Here is an argument: Simulation can avoid wasting of time and money. With its inherent iterative power, SPICE covers numerous application cases in which you could easily detect any design flaw or product weakness. The stability of a closed-loop SMPS represents a typical application when some key feedback elements are moving (that is, the

variable load that affects a pole), or start to degrade with temperature and aging (as the electrolytic Equivalent Series Resistor). Moreover, design ideas can also be tested or assessed in a snapshot through a computer and, if they are worth the shot, be further refined in the lab.

2. Simulate test measurements whenever you do not own the adequate equipment: a high-voltage floating probe (in bridge applications), a network analyzer (to evaluate an SMPS bandwidth), and so on.
3. Power libraries are safe: they let you experiment "what if" when amps and kV are flowing in the circuit without explosion in the case of a wrong connection!

What You Will Find in the Following Pages

The advantages of the power of SPICE are thoroughly detailed in this book. This will help you understand, simulate, test, and finally improve the *Switch-Mode Power Supply* (SMPS) you want to design. By providing you with specific simulation recipes, this work intends to facilitate as much as possible for your SMPS design stage and in particular, in the following areas:

- AC responses with average, small, or large signal models
- Breadboard like simulations with generic transient models
- Writing the model of your own switch-mode controller
- Audio susceptibility, output impedances measurements, and so on in voltage-mode or current mode
- Effects of leakage elements, clamp calculation, and so on.

The first chapter explains how *average* models were derived. A good comprehension of this chapter is fundamental; it will help you question weird SPICE data, resulting from a bad model implementation. If you do not understand the way the model has been derived, you will obviously face some difficulties in solving these issues. In this chapter, you will also learn the way to wire an average model and run basic simulations. Since every integrated IC does not always come with a SPICE model, Chapter 2 will describe how the generic *switched* models were derived. The reading of this chapter will interest the reader who wants to strengthen his knowledge in SPICE model writing. The remaining chapters give you the recipes to apply

if you want to simulate standard topologies by combining the averaged and switched models previously described.

When discussing SPICE simulations, one of the greatest issues takes root in the version syntax. Most SPICE editors deal with a proprietary syntax, sometimes SPICE3 conformant, that makes translation from one platform to another a difficult and painful exercise. To allow the use of different simulators, the standard models presented throughout the pages are compatible with Intusoft IsSpice (San-Pedro, CA), CADENCE's PSpice (Irvine, CA), and Spectrum Software's Micro-Cap (Sunnyvale, CA). From time to time, some specific key syntax will also be declined into a different platform (or SPICE revision) to help you make a translation whenever needed.

To help you quickly copy/paste the examples, we have included a CD-ROM in this book. The entire Chapter 3 simulation templates are offered in IsSpice/PSpice/Micro-Cap syntax, and you can easily load them onto your computer if you are equipped with one of these softwares. For students or newcomers to the SPICE world, we have included the demonstration versions of these editors. They let you open the aforementioned files and simulate some of them (those demos are size limited) to give you a taste of what the full version can do. In the very last portion of this book, we introduce PSIM from Powersim Technologies (Canada), which has specifically been developed for power electronic circuits. A working demo version is also part of the CD.

What You Will NOT Find in This Book

This book does not describe the way that SPICE operates, neither does it solve typical electrical circuits. It assumes that the reader is already familiar with the basics of SPICE simulations. Numerous books and papers are available on the subject, as the bibliography details [27, 30, 31]. Similarly, the author will not spend too much time on the description of the studied topologies. Whenever possible, the extended bibliography will guide your choice if you wish to strengthen your knowledge on a particular domain [15, 20, 21]. If some of the theoretical results are sometimes delivered "as is," we strongly encourage the reader to further dig into the appropriate literature and acquire the theory that precedes the result.

The book also only focuses on a system approach. No SPICE description of typical discrete power elements such as diodes, MOSFETs, and so on is proposed.

After this brief introduction, it is time to plunge into the intricacy of the SMPS SPICE simulations.

What Kind of Models Are Available?

Any SMPS is made of switching elements (MOSFETs, diodes, IGBTs, and so on) and storage components (inductors and capacitors). The way you arrange these elements together leads you to a given *topology*. We can define three *basic* topologies from which others are derived:

- The **BUCK**: Use this converter when you need to have an output voltage *lower* than the input one, without any galvanic isolation. An extension from this first topology is the FORWARD converter, which combines a transformer to provide the end user with isolation. Further extensions are possible, like the half-bridge, the full-bridge, and the push-pull. In these devices, the energy transfer takes place during the time the main switch is closed.
- The **BOOST**: This topology will make the output voltage *higher* than the input one. There is no galvanic isolation.
- The **BUCK-BOOST**: When you need to either *decrease* or *elevate* the output voltage, the BUCK-BOOST is a possible choice, but to the penalty of a *negative* output voltage (by reference to the input ground). To overcome its lack of isolation, the FLYBACK topology can be used, this time without any polarity restrictions. In these two last converters, the input to output energy process occurs at the switch opening.
- The **Single Ended Primary Inductance Converter (SEPIC)**: The Single Ended Primary Inductance Converter finds high-volume applications in portable handsets (for example, GSM phones) where you need to either *boost* or *decrease* the battery voltage *without* inverting the output voltage.

Each basic topology requires an independent model that can be expanded by the adjunction of an external transformer to generate FORWARDs, FULL-BRIDGE, etc., and so on. We will describe each model separately in the coming pages. However, depending on the performance or defaults you wish to highlight, two different model approaches are at your disposal: *average* models or *switched* models.

A *switched* model is a way to simulate the behavior of an electrical circuit exactly as if you were building it on a breadboard. The semiconductor models, the transformer, its associated leakage elements, the peripheral elements, and so on will be included. In this case, the time variable **t** is of primary importance because it governs the overall circuit operation and performances such as semiconductor losses, ringing spikes due to parasitic, and stray elements, and so on. Because SMPS usually works at high frequencies, the simulation of response times in the order of milliseconds can be computationally high, leading to prohibitive analysis times. Keep in mind that SPICE acts like a sample-and-hold system that continuously adjusts its internal timestep depending on the dI/dt or dV/dt the analyzed circuit is the seat of. Furthermore, transient analysis does not easily lend itself to AC transfer function evaluations.

On the other hand, *average* models represent a method in which the switching component has disappeared in favor of a unique state equation describing the average behavior of the system; in a switching system, a set of *linear* equations describes the circuit's electrical characteristics for the two *stable* positions of the ON or OFF switch(es) (Figure 1-1d for a BUCK converter). Please note that a third interval also exists when the converter leaves the *Continuous Conduction Mode* (CCM) and then enters the *Discontinuous Conduction Mode* (DCM). How do you properly link the two (or three in DCM) matrixes? A method such as the *State-Space-Averaging* (SSA) technique, (introduced by Middlebrook and Cùk in the 1980s, [1]) consists in smoothing the discontinuity associated with the transitions of the switch(es) between these states. The result is a set of continuous *nonlinear* equations in which the state equation coefficients now depend upon the duty cycles ***d*** and ***d'*** (1-*d*). A linearization process around a stable operating point finally leads to a set of *continuous linear* equations. The reader interested by an in-depth description of these methods will find all the necessary information in a very instructive book written by D. M. Mitchell [2]. As we will further see, the SSA is a) a long and rather complicated process b) a long process because you restart from scratch every time you modify the converter's configuration (for example, when you add an input filter). Fortunately, as the following paragraphs describe, the SSA is not the unique method in effect to deliver the small-signal characteristics of a type of converter.

Following are the advantages and drawbacks of both model types.

Average Models

- Small-signal response: Draw Bode or Nyquist plots in a snapshot and assess the stability.
- Input and output impedance plots: In the first case, verify the stability when adding an input filter.
- No switching component: Simulation results are immediate.
- You can visualize long, transient effects of several tens milliseconds. (for example, in a low bandwidth system like a Power Factor Corrector).
  - It is difficult to see the effects of parasitic elements, although some good models now include them.
  - You cannot evaluate the switching losses of semiconductors.

Transient Models

- They can include parasitic elements: See the effect of the leakage inductance and quantify the main switch voltage stress or the poor resulting cross-regulation.
- Propagation delays can be accurately modeled: What is my real final peak current when it takes 150ns to fully propagate the internal latch reset and finally open the power switch?
- Ripple levels and sampling effects are easily revealed by transient simulations.
- You can precisely evaluate *conduction* losses, RMS, Average levels, etc.
  - Because of the numerous switching events, the simulation time can be very long.
  - Transient response is difficult to assess in low-bandwidth applications.

The following paragraphs briefly detail how most known average models can be used or derived. We deliberately emphasized the latest model description (GSIM) because this is the one we will principally use.

Understanding What *Averaged* Quantity Means

As you will discover in the following chapters, several options exist to model or derive the small-signal equivalent circuit of a given topology: a) you either write the state equations corresponding to the two switch(es) positions and average them over a switching cycle, or b) you directly average the converter waveforms. The common denominator of those methods remains the final small-signal linearization needed to extract the equivalent model. The first method, a), is described through the *State-Space Averaging* (SSA) technique, while the other options include circuit averaging and averaged switch modeling.

To clarify the concept, let us explain what "averaged" means: this usually means that a period of a periodic time function (for example, the switch current in a converter) is integrated during a cycle and divided by the duration of that cycle. Thus, the averaged function is a succession of separate discrete values. If you replace that discrete function with a continuous function that has the same values as the averaged function at the end of each period and is essentially smooth, then you get an "averaged and continuous" representation of the original function. This concept is described in Figure 1-1a. You see how a waveform, for instance, the duty-cycle evolution in an AC modulated converter, is smoothed over the discrete average values. The duty-cycle is modulated following the law $d(t) = D_{DC} + D_m . \cos\omega_m t$. D_{DC}, which represents the steady-state duty-cycle corresponding to a given operating point. Both D_{DC} and D_m are constant with the condition $|Dm| << D_{DC}$ implying that the system under study stays linear in the modulated region. Finally, the modulation frequency ωm is much smaller than the converter switching frequency. The averaged and continuous function is similar to the filtered waveform, but is not exactly the same, because it is a mathematical abstraction rather than a real time-dependent physical variable. As Figure 1-1a shows, the ripple has been neglected.

In the average circuit modeling technique, the exercise lies in isolating and replacing the switch network with a set of current and voltage sources whose electrical architecture do not vary with time. If we take the example of the BOOST converter, we can redraw its electrical schematic highlighting the aforementioned sources, now called $v_1(t)$ and $i_2(t)$; Figure 1-1b depicts this concept.

When the switch closes during the ON time (or d.Ts), $v_1(t) = i_2(t) = 0$. At the switch opening (during d'.Ts), $v_2(t)$ appears across its connections because of the diode conduction and $i_2(t) = i_1(t)$. Figure 1-1c graphically represents these waveforms. Now let us average the signals over a switching cycle:

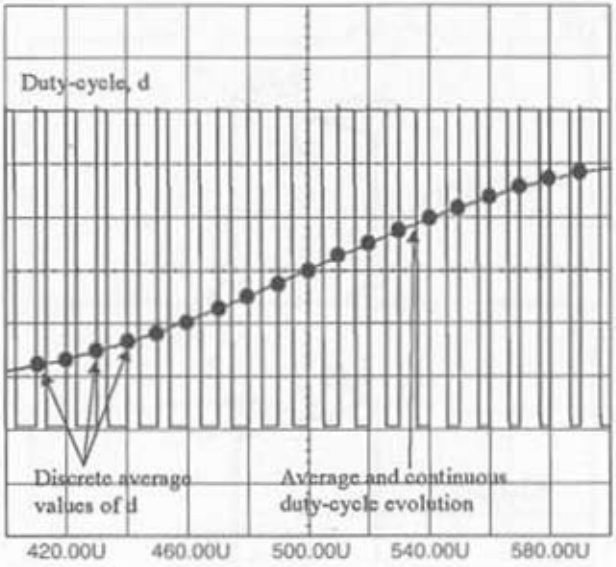


Figure 1-1a
When discrete averaged values are smoothed, you obtain a continuous representation.

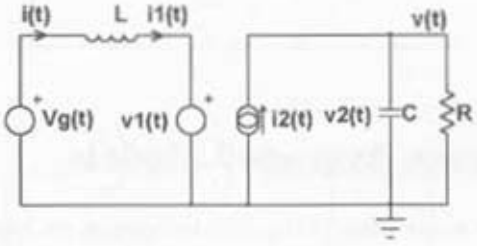


Figure 1-1b
The switch network is replaced by two time-dependent generators.

$$< v_1(t) >_{Ts} = \frac{1}{Ts} \cdot \int_0^{Ts} v1(t).dt = d'(t) \,.\, < v_2(t) >_{Ts}$$

$$< i_2(t) >_{Ts} = \frac{1}{Ts} \cdot \int_0^{Ts} i2(t).dt = d'(t) \,.\, < i_1(t) >_{Ts}$$

By plugging these averaged equations into the Figure 1-1b model, we obtain a nonlinear circuit-averaged model for the BOOST converter. The next step would consist in perturbing and linearizing the equations to extract the final small-signal model and its electrical representation. Reference [21] thoroughly covers all of these important modeling aspects, including current-mode and resonant switches.

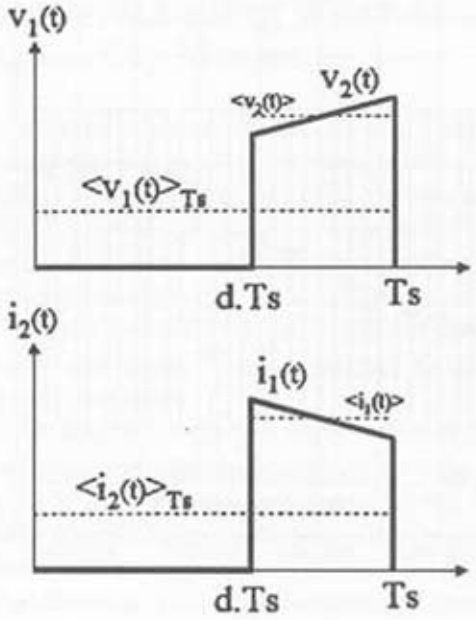


Figure 1-1c
The time-dependent generator waveforms are made identical to those of the original BOOST.

State Space Averaged Models

To give you a small taste of the SSA technique, we have presented a simple BUCK converter and highlighted the *state* variables. State variables are usually associated with storage elements like capacitors and inductors. If we know the state of these variables at a given time, (for example, at $t = 0$) then we should be able to solve the system equations for other $t > t_0$. (See Figure 1-1d.)

You first need to write the classical node/mesh equations, then rearrange them to reveal the state variables: x1 the inductor current and x2 the capacitor voltage. You have as many state variables as storage elements (the number of storage elements also directly gives the order of the circuit). The object of the development is to make the equations fit the universal format: $\dot{x}(t) = A_j x(t) + B_j u(t)$ where $\dot{x}(t) = \dfrac{dx(t)}{dt}$ (eq. 1.1); A is called the state coefficient matrix and B represents the source or input coefficient matrix. As previously stated, we make the distinction between two switching cases (assume we are in CCM):

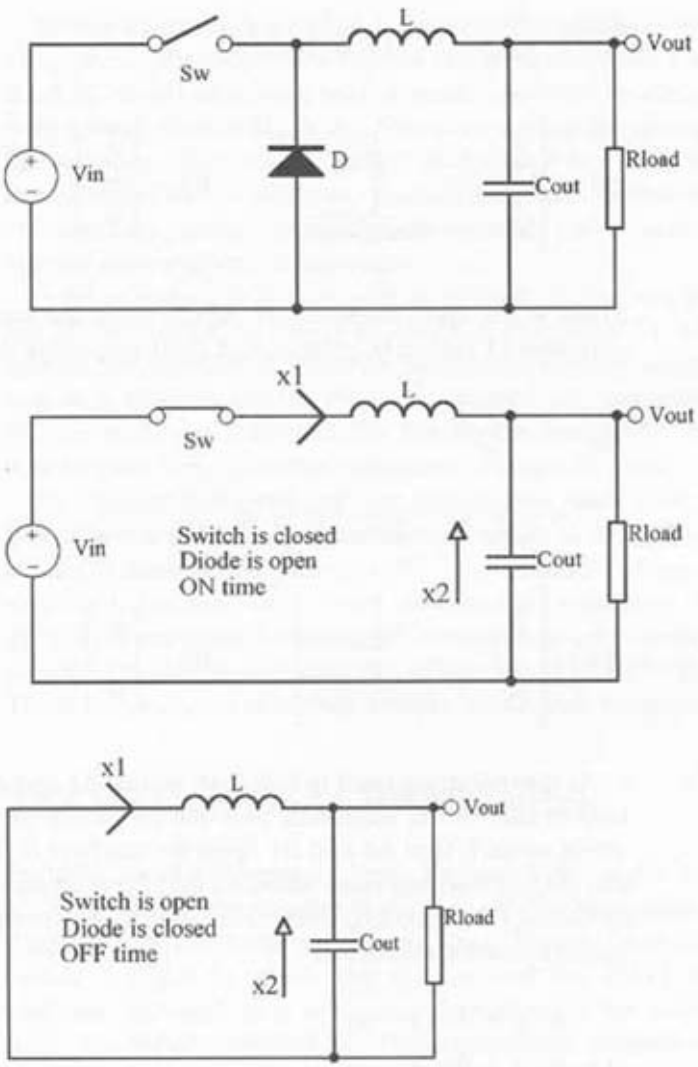


Figure 1-1d
SSA requires to write the equations over the entire electrical network during the switch states.

State 1: Sw closed, diode open. Solve the equation with the state variables x1 and x2 in order to find their respective derivatives:

$$\frac{dx1}{dt} = -\frac{1}{L} \cdot x2 + \frac{1}{L} \cdot vin \qquad \text{(eq. 1.2)}$$

$$\frac{dx2}{dt} = \frac{1}{Cout} \cdot x1 - \frac{1}{Rload.Cout} \cdot x2 \qquad \text{(eq. 1.3)}$$

$$A1 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{Rout.Cout} \end{bmatrix} \qquad B1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

State 2: Sw open, diode closed. Again, solve the equation with the state variables x1 and x2 in order to find their respective derivatives:

$$\frac{dx1}{dt} = -\frac{1}{L}x2 \qquad \text{(eq. 1.4)}$$

$$\frac{dx2}{dt} = \frac{1}{Cout}x1 - \frac{1}{Rload.Cout}x2 \qquad \text{(eq. 1.5)}$$

$$A2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{Rout.Cout} \end{bmatrix} \qquad B2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

At this point, we need to link both states: A1 and A2, B1 and B2. If you look at the BUCK schematic and the equations we wrote, you certainly would remark that A1 and B1 apply for the first (ON) interval, or during dth of the switching time, while A2 and B2 exist during the *(1-d)*th (OFF) switching time interval. Using this remark, we can combine both matrixes by the following equations:

$$A = A1.d + A2.(1 - d) \qquad \text{(eq. 1.6)}$$

$$B = B1.d + B2.(1 - d) \qquad \text{(eq. 1.7)}$$

These equations would be linear if d and *(1-d)* were constant. However, in a normal application, this is not the case because some of the state variables (x2 in our BUCK) are fed back to a control IC. This chain continuously adjusts d in order to keep the output voltage constant. In sum, we have transformed a set of two distinct linear equations into a set of *nonlinear* but *continuous* equations. However, keep in mind that this SSA process holds only if the time constants of the circuit are very large compared to the switching frequency.

To end the process, we need to linearize the system across a given operating point. Classically, we replace the variables with a static portion (a fixed DC level) associated with a small amplitude modulation (also noted with a small ^): $d \rightarrow D_{DC} + d_{AC}$. The same applies for the input voltage and the state variables. An equivalent small-signal is further derived and you can calculate all the necessary transfer functions. Reference [2] documents the complete process (including current-mode converters), and we encourage the reader to read it thoroughly.

A bit of historical background: In 1978, R. Keller was the first to apply the Middlebrook/Cùk theory to a SPICE simulator [3]. AT this time, the models developed by R. Keller required some manual computation of parameters in order to provide the simulator with key information such as the DC operating point, for instance. Finally, the simulation was only valid for small signal variations and continuous conduction mode.

Dr. Vincent Bello was the first person, two years later, to port Middlebrook's nonlinear state-space averaged models to the SPICE domain [4]. In BELLO's models, the previous AC cross-products terms were no longer neglected. Instead, they were dynamically multiplied by some *POLY* SPICE2 statements. Large-signal variations could then be simulated that allowed the user to visualize the effects of a 0 to 100% duty-cycle sweep. These *Large-Signal Models* (LSM) are best suited for Transient runs.

The Voltage-Mode PWM Switch

In 1986, Vatché Vorperian, from Virginia Polytechnic Institute (VPEC, USA), developed the concept of the *Pulse Width Modulation* (PWM) switch model [5]. At about the same time, Larry Meares from Intusoft also presented a paper in which the approach of the PWM switch was also explored, although in a less comprehensive manner since CCM was the only case Meares covered [6]. These gentlemen considered modeling the power switch alone (averaged switch modeling technique) to finally insert an equivalent small-signal, three-terminal model (nodes A, P, and C) into the converter schematic: exactly the same way as when you study the transfer function of a bipolar amplifier. The analysis is considerably simplified given that no more average or linearization process is required; put the small-signal model in place and solve the equations to derive the parameters of your choice! With this method, Vorperian demonstrated, among other results, that the Flyback converter operating in DCM was still a second-order system, affected by a high-frequency Right-Half Plane zero. This result was not correctly predicted by SSA; the third interval in DCM

(the deadtime) causes the state variable x1 to disappear. People considered the BUCK or BUCK-BOOST to be a true first-order system. However, as reference [8] details, a recent reexamination of the original SSA process leads to slightly different results compared to those found by Vorperian and Meares.

Since its introduction, the PWM switch has not been the object of many publications in specialized press, and some designers may think that its use is only reserved to modeling experts. Because its implementation is easy and powerful, we will go through a short example, but without entering into the details of its electrical origins.

The simplified small-signal PWM switch model operating in CCM is presented in Figure 1-2a.

To highlight its use, we will stick to reference [5]'s BOOST example, which appears in Figure 1-2b. In the following example, we will study the DC input audiosusceptibility $\frac{Vo}{Von}$ or using Vorperian's notation: $\frac{Vo}{Vg}$. For that purpose, the sources related to the *dynamic* duty-cycle "d" disappear and only the static DC values are kept in place (D and D'). If you wish to detail the transfer function $\frac{Vo}{d}$, simply put these sources back to the schematic and solve for the equations.

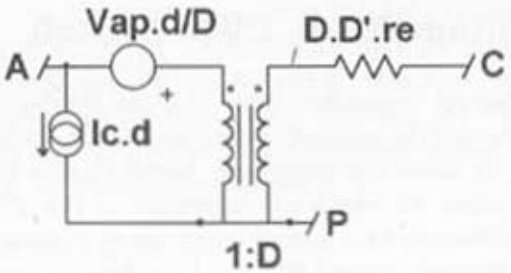


Figure 1-2a
The PWM switch DC model.

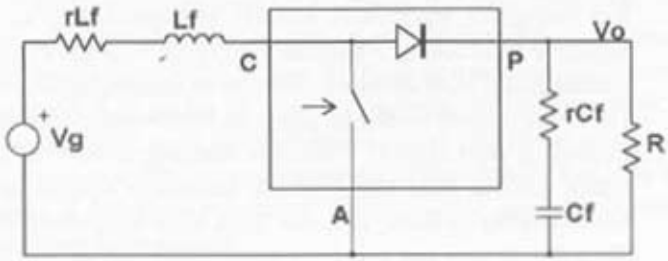


Figure 1-2b
A way to wire the three-terminal model in order to evaluate the BOOST characteristics.

When SPICE computes the DC point of any circuit, it first removes the capacitors and shorts the inductors. We will apply the same technique to Figure 1-2b while wiring the PWM model depicted by Figure 1-2a. The result appears in Figure 1-2c, where

rCf = output capacitor's ESR

rLf = inductor series resistor

re = R // rCf

D' = 1-D

R = output load

Vg = input voltage

Different approaches exist to solve this kind of circuit where the transformer is not commonly wired: the classic brute force approach, using nodal and loop equations, or the soft approach that consists of transforming the schematic until a well-known structure is found. Generally speaking, the first method usually leads to correct but abstruse results in which the action of a component inside the considered function is not obvious. Inversely, the soft method produces so-called low-entropy expressions [7] and yields insight into the circuit under study.

Let us adopt the second method, thus redrawing a simplified version of Figure 1-2c as represented in Figure 1-3a.

We first mark the currents, keeping in mind that a current entering a winding by a dot leaves the coupled winding by the other dot in the same direction.

The Vo/Vg transfer function is easily obtained after a few lines:

$$Vg - V1 = Vo$$

$$V1 = -Vo \cdot D$$

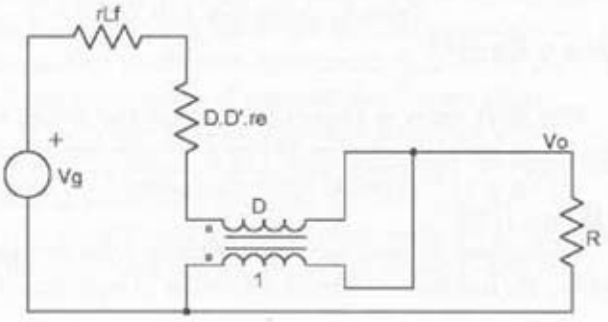


Figure 1-2c
The final BOOST DC model reduces to a simple electrical circuit.

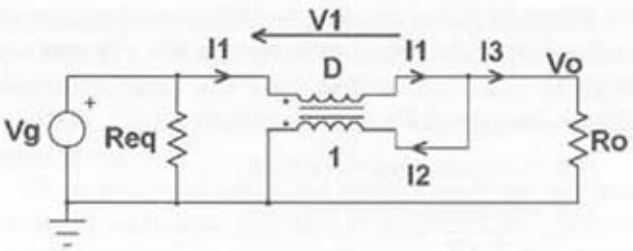


Figure 1-3a
The intermediate step helps us understand how the circuit operates.

$Vg + Vo \cdot D = Vo$

$Vg = Vo - Vo \cdot D$ so $Vo/Vg = 1/(1 - D)$ or $\mathbf{Vo/Vg = 1/D'}$ (eq. 1.8)

The input impedance, or the way Ro is reflected across Vg (Req), is also simple to derive:

$N1.I1 = N2.I2$. Because $I1 = Vg/Req$, it is possible to write the following

$$N1 \cdot Vg/Req = N2.I2.$$

From Kirchhoff's law, $I2 = I1 - I3$, with $I3 = Vo/Ro$

By definition, $N1 = D$ et $N2 = 1$

$$D \cdot Vg/Req = Vg/Req - Vo/Ro$$

$$D \cdot Vg/Req = (Vg \cdot Ro - Req \cdot Vo)/(Req \cdot Ro).$$

Simplifying by Req:

$$D \cdot Vg = Vg - (Req \cdot Vo)/Ro$$

$$Vg/Vo \cdot (1 - D) = Req/Ro.$$

From equation (eq. 1.8) $Vg/Vo = 1 - D$, so:

$\mathbf{Req = Ro \cdot D'^2}$ (eq. 1.9)

The I3/I1 ratio is important to feed the model with its DC operating points as we will later see. If Pin = Po, one can write $Vg.I1 = Vo.I3$, so $I1/I3 = Vo/Vg = 1/D'$. Back to Vorperian's model of Figure 1-2b, $\mathbf{Ic = -I1 = -Io / D'}$ (eq. 1-10).

With these simple formulas, Figure 1-3b represents our DC BOOST where Ro has been reflected according to equation (1.9):

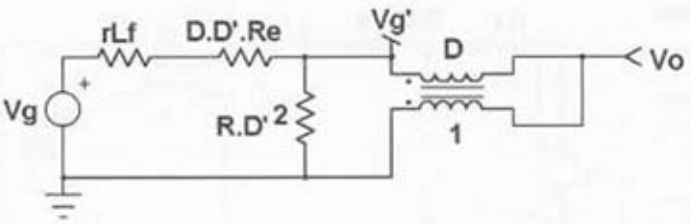


Figure 1-3b
This final intermediate step unveils the BOOST DC function.

We are in the presence of a simple resistive divider whose output Vg' undergoes a 1/D' multiplier ratio (1.8). Thus, the DC Vo/Vg transfer function is really straightforward. So, after factoring the $R \cdot D'^2$ term

$$\frac{Vo}{Vg} = \frac{1}{D'} \cdot \frac{1}{1 + \frac{rLf}{D'^2 \cdot R} + \frac{re \cdot D}{R \cdot D'}} = M \qquad \text{(eq. 1.11)}$$

Now, let's turn into AC analysis or audio susceptibility (how Vout varies when Vin moves). We put the capacitors and inductors in place, as Figure 1-4a shows.

This structure is still not very convenient. For the next step, we will reflect all the components located on the right side of Figure 1-4a to the "primary" side of the transformer. It is easy with equation (1.9).

Figure 1-4b reveals a classical LC filter affected by its parasitic elements, once again followed by a 1/D' multiplier. Since we want to obtain the Vo/Vg transfer function but also the input or output impedances (further noted Z_{in} and Z_{out}) parameters of this circuit, a good method is to use matrix algebra. Matrix algebra is well suited for numerical computations on a computer, and SPICE makes an extensive use of it. It is true that the symbolic answer given by a transfer matrix does not give the designer much insight into the circuit's operation. However, one remarkable point is that once you found the matrix coefficients, the resulting transfer matrix contains, in one shot, all the parameters of interest (see Figure 1-5a).

If matrixes require constant attention when you manipulate them by hand, it becomes child's play when you use some mathematics programs such as Mathsoft's Mathcad (Cambridge, MA).

To solve Figure 1-4b's problem, we draw a simplified schematic of the LC filter (Figure 1-5b) where we put state (x) and output variables (y).

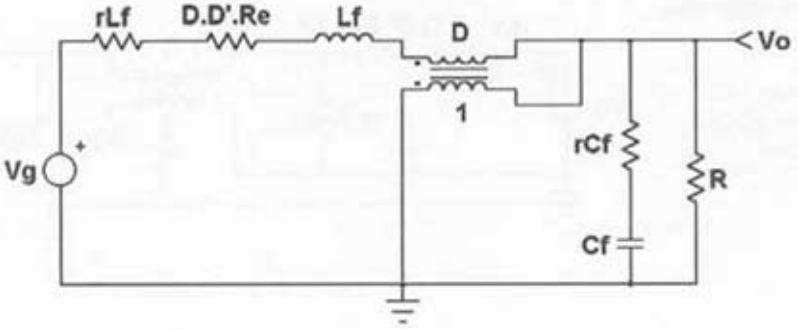


Figure 1-4a
To obtain the AC transfer function, the storage elements are back to the schematic.

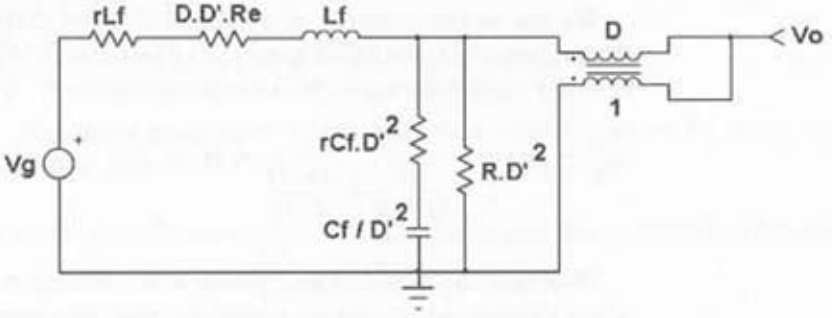


Figure 1-4b
Reflecting rCf and Cf to the transformer's primary reveals a more friendly structure.

$$T(s) = \begin{bmatrix} \frac{Y1(s)}{U1(s)} & \frac{Y1(s)}{U2(s)} \\ \frac{Y2(s)}{U1(s)} & \frac{Y2(s)}{U2(s)} \end{bmatrix} \quad T_{1,1} = Z_{in},\ T_{2,1} = V_o/V_g,\ T_{2,2} = Z_{out}$$

Figure 1-5a
A transfer function matrix gives all the relevant parameters in one shot.

Theory dictates that the generalized transfer function T(s) of a n^{th} order *linear* passive system is: $T(s) = [M\,(sI\text{-}A)^{-1}\,B + N]$ (1.12), where A and M are the state coefficient matrixes, B and N the source coefficient matrixes [2]. The steps will be to write the state and output equations, ordered as follows:

State equations

$$x1 = \frac{1}{L}\cdot\left[R1 + \frac{R2\cdot R3}{(R2+R3)}\right]\cdot x1 + \frac{1}{L}\cdot\left(\frac{R2}{R2+R3} - 1\right)\cdot x2 + \frac{1}{L}\cdot u1 - \frac{1}{L}\cdot\frac{R2\cdot R3}{R2+R3}\cdot u2$$

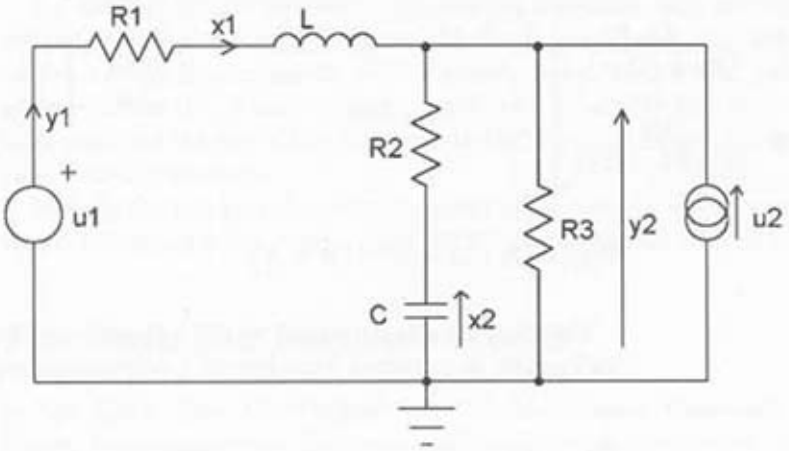


Figure 1-5b
A simplified version of Figure 1-4b circuit eases the math expressions.

$$x2 = \frac{R3}{(R2 + R3)\cdot C}\cdot x1 - \frac{1}{C\cdot(R2 + R3)}\cdot x2 - \frac{R3}{C\cdot(R2 + R3)}\cdot u2$$

(eq. 1.13) (eq. 1.14)

Output equations

$$Y1 = x1$$

$$Y2 = x1\cdot R3\cdot\left(1 - \frac{R3}{R2 + R3}\right) + \frac{R3}{R2 + R3}\cdot x2 + u2\cdot R3\cdot\left(1 - \frac{R3}{R2 + R3}\right)$$

(eq. 1.15) (eq. 1.16)

Now feed Mathcad with these coefficients and write the generalized equation as depicted by (1.17):

$$A = \begin{bmatrix} -\dfrac{R1\cdot R2 + R1\cdot R3 + R2\cdot R3}{(R2 + R3)\cdot L} & \dfrac{-R3}{(R2 + R3)\cdot L} \\ \dfrac{R3}{(R2 + R3)\cdot C} & -\dfrac{1}{C\cdot(R2 + R3)} \end{bmatrix} \quad M = \begin{pmatrix} 1 & 0 \\ \dfrac{R3\cdot R2}{R2 + R3} & \dfrac{R3}{R2 + R3} \end{pmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L} & \frac{-R2 \cdot R3}{(R2 + R3) \cdot L} \\ 0 & \frac{R3}{C \cdot (R2 + R3)} \end{bmatrix} \qquad N = \begin{pmatrix} 0 & 0 \\ 0 & \frac{R2 \cdot R3}{R2 + R3} \end{pmatrix}$$

$$T(s) = [M \cdot (sI - A)^{-1} \cdot B + N] \qquad \text{(eq. 1.17)}$$

The final results delivered by the software are in a clear ordered form. Vo/Vg ratio is extracted from Figure 1-5a's matrix transfer, T_{21}:

$$\frac{Vo}{Vg} = \frac{1}{D'} \cdot \frac{R3}{R1 + R3} \cdot$$

$$\frac{1 + s \cdot C \cdot R2}{s^2 \cdot L \cdot C \cdot \left(\frac{R3 + R2}{R1 + R3}\right) + \left[s \cdot \frac{L + C \cdot (R2 \cdot R3 + R3 \cdot R1 + R1 \cdot R2)}{R1 + R3}\right] + 1} \qquad \text{(eq. 1.18)}$$

After replacing the elements by Figure 1-4b's values and putting the equation into a second order form, we extract the first zero s_{z1} and the tuning frequency ω_0:

As previously calculated, $M = (1 / 1 - D) \cdot R3 / (R1 + R3)$ (eq. 1.19)

Second-order general function: $\frac{1}{\left(\frac{s}{\omega o}\right)^2 + \frac{s}{\omega o \cdot Q} + 1}$ (eq. 1.20)

After identifying:

1st zero: $\omega_{z1} = 1/R2 \cdot C$ (eq. 1.21)

Tuning frequency:

$$s^2 \cdot L \cdot C \cdot (R2 + R3)/R1 + R3 = s^2/\omega_0^2 \rightarrow \omega_0 =$$

$$\frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{R1 + R3}{R2 + R3}} = \frac{1}{\sqrt{L \cdot C}} \cdot \sqrt{\frac{rLf + re \cdot D \cdot D' + D'^2 \cdot R}{rCf + R}} \qquad \text{(eq. 1.22)}$$

Z_{in} and Z_{out} can be immediately deducted the same way. To obtain the Vo/d AC transfer function, you now add the dynamic sources (Figure 1-2a) and rearrange the schematic until a known structure is found, exactly as we previously did. *Discontinuous Conduction Mode* (DCM) study would have required the use of the appropriate PWM switch model, but the principle remains the same.

Despite the fact that the primary intent of Vorperian's model was educational, his model lends itself well to SPCE simulations as we will later see.

The Switched Inductor Model

In the 1990s, Sam Ben-Yaakov from the Ben-Gurion University of the Negev (Israel) introduced the concept of the *Switched Inductor Model* (SIM) [9]. His approach is similar to the PWM switch concept except that Ben-Yaakov includes the inductor as part of his model. As a first result, his model is topology independent. If you look at the following pictures (Figure 1-6), you certainly notice they all share a common switching system, which is topology independent. The switch actually plays the role of a *single-pole double-throw device* (SPDT).

It routes the current of one inductor end to two other terminals (b, c), depending on the switching interval, ON or OFF. Figure 1-7a details the idea.

If you consider the *instantaneous* inductor current $\frac{dIL}{dt}$ to be $\frac{VL}{L}$, then the derivative of the average inductor current becomes $\frac{|V_L|}{L}$ (eq. 1.23). With that expression in mind, it is easy to write that the *total average* voltage across the inductor is the sum of both ON and OFF average voltages: $\overline{VL} = Vab \cdot D_{ON} + Vac \cdot D_{OFF}$ (eq. 1.24), D_{ON} and D_{OFF} being the respective duty-cycles for the ON and OFF intervals. This statement holds for both CCM and DCM, because in the latter case, there is no more current flowing through the inductor during the third interval, hence no voltage.

Since our inductor acts as a set of three dependent current generator (the real inductor current, I_L, the ON and OFF time current), Figure 1-7b gathers them into the *Generic Switched Inductor Model* (GSIM), which represents the foundations of the eponymous average models.

Figure 1-7b implements *averaged* current generators whose values are defined according to the *averaged* inductor current. A simple electrical circuit generates this inductor current using the fact that $\frac{\overline{dI_L}}{dt} = \frac{\overline{V_L}}{L}$. By gen-

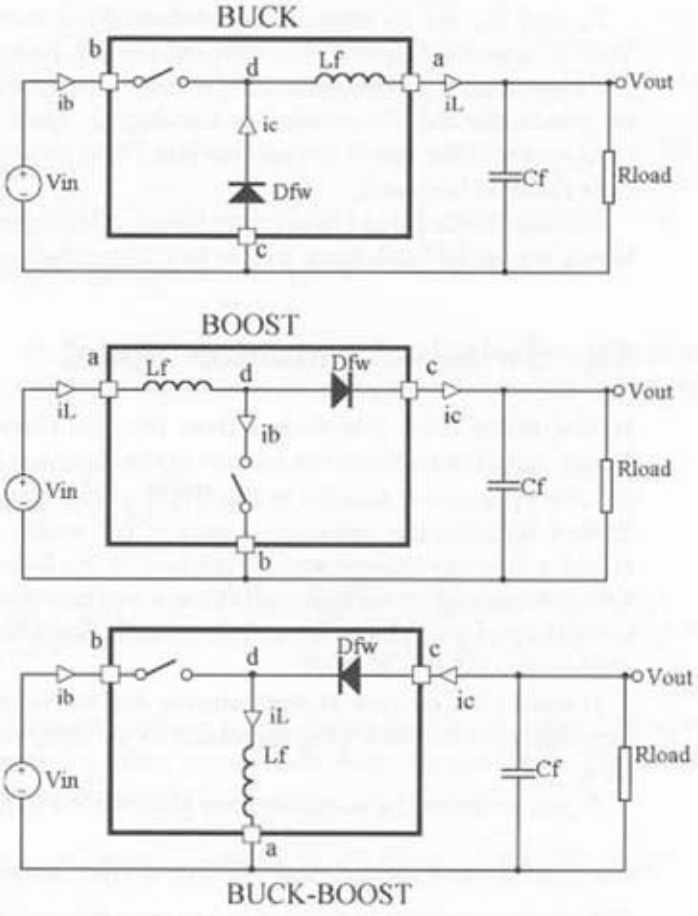


Figure 1-6
During the switch commutation, the inductor voltage is a function of V(a,b) and V(a,c).

erating V_L according to equation (1.24), we apply this level across the real inductor Lf and its series resistor, thus forcing the desired level. A dummy voltage source acts as the current sensor to evaluate I(L). However, depending on the operation mode, CCM or DCM, this average value will considerably change. A look at Figures 1-7d (CCM) and 1-7e (DCM) shows the differences between both modes values.

In DCM, the third interval DT expands the OFF time and prevents the switch from immediately turning on again. In CCM, DT does not exist. The OFF time D' or D_{OFF} is therefore linked to the duty-cycle D or D_{ON} by D' = 1 − D. We can rewrite the relation as $D_{OFF} + D_{ON} = 1$, which means the

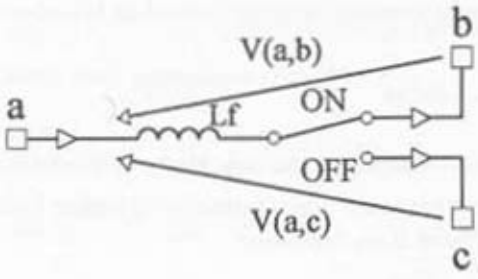


Figure 1-7a
The power switch routes the inductor current to terminals b and c, depending on the interval.

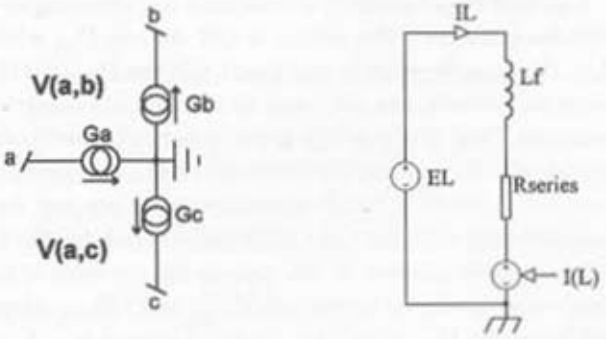


Figure 1-7b, Figure 1-7c
These diagrams represent the foundations of the GSIM model.

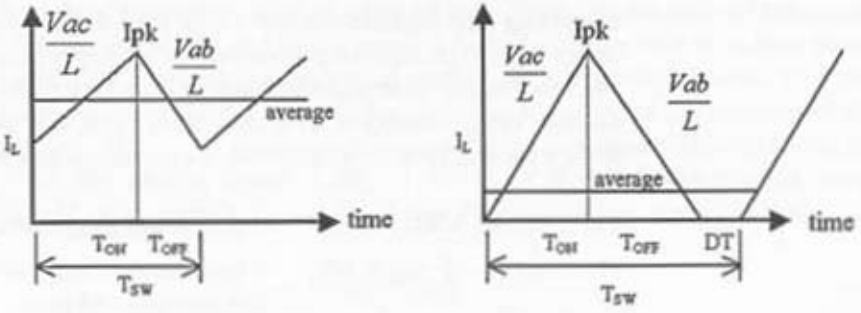


Figure 1-7d, Figure 1-7e
Inductor current shapes reveal different average current in CCM (1-7d) or DCM (1-7e).

system is operating in CCM (DT = 0). If we are in DCM, this relationship no longer holds and we have $D_{OFF} + D_{ON} + DT = 1$ or $D_{OFF} + D_{ON} < 1$. By using these definitions, we will build a model that automatically toggles from one mode to the other by monitoring the DON + DOFF sum.

The one-cycle average value compared to Ipk also reveals the operating mode:

- $\overline{I_L} < \frac{Ipk}{2} \rightarrow DCM$
- $\overline{I_L} = \frac{Ipk}{2} \rightarrow$ Critical Conduction Mode, or borderline operation (BCM)—the current ramps-up again immediately after hitting 0. We are well in DCM but there is no deadtime.
- $\overline{I_L} > \frac{Ipk}{2} \rightarrow CCM$

D_{ON} and D_{OFF} normally correspond to percentages: the percentage of the switching period T the switch is ON defines D_{ON} while the rest of the time $(1 - D_{ON})$ can be shared by D_{OFF} (CCM) or D_{OFF} + DT (DCM). To cope with electrical simulators, we need to manipulate electrical variables, not percentages. That is why a 100 percent duty-cycle will often be defined by a 1V signal. All value below 1V illustrates the intermediate steps down to 0 percent: for example, 680mV represents a 68 percent duty-cycle. This remark does not only hold for the GSIM models but for the vast majority of available *averaged* models. In the remaining portions of text, D_{ON} and D_{OFF} will thus respectively be coded into VD_{ON} and VD_{OFF} voltage generators. As you will later see, D_{ON} is imposed by the feedback loop (usually the error amplifier), while D_{OFF} is internally computed by the model.

Deriving the Equations for CCM and DCM Let us now first separately define the current generators for both operating conditions. In CCM, the relationship is straightforward. Figure 1-7b speaks for itself. To be consistent, VD_{ON} actually represents a duty-cycle, but is encoded into voltage to fit with the SPICE primitive G, a current-controlled source:

$Ga = \overline{I_L}$ (eq. 1.25) → this is the total *average* inductor current

$Gb = VD_{ON} \cdot \overline{I_L}$ (eq. 1.26) → the *average* inductor current circulates during the ON time

$Gc = VD_{OFF} \cdot \overline{I_L}$ (eq. 1.27) → the *average* current circulates during the OFF time

$VD_{OFF} = 1 - VD_{ON}$ (eq. 1.28) → there is no deadtime in CCM

In DCM, the average value can be found by looking at Figure 1-7e. The total area is the sum of the ON area and the OFF area. The ON area is sim-

ply $\frac{Ipk \cdot t_{ON}}{2}$ (eq. 1.29), while the OFF area is $\frac{Ipk \cdot t_{OFF}}{2}$ (eq. 1.30). Summing both expressions leads to

$$Ga = \overline{I_L} = \frac{VD_{ON} + VD_{OF}}{2} \cdot \overline{Ipk} \text{ (eq. 1.31)}$$

$$Gb = \frac{VD_{ON}}{2} \cdot \overline{Ipk} \text{ (eq. 1.32)} \quad \rightarrow \text{the average inductor current during the ON time}$$

$$Gc = \frac{VD_{OFF}}{2} \cdot \overline{Ipk} \text{ (eq. 1.33)} \quad \rightarrow \text{the average inductor current during the OFF time}$$

The continuous smoothed peak current can be defined by

$$\overline{Ipk} = \frac{\overline{V(a,b)} \cdot VD_{ON}}{L} \cdot Tsw = \frac{\overline{V(a,c)} \cdot VD_{OFF}}{L} \cdot Tsw \text{ (eq. 1.34), with Tsw as}$$

the switching period. From this equation we easily extract VD_{OFF} by

$$VD_{OFF} = \frac{VD_{ON} \cdot \overline{V(a,b)}}{\overline{V(a,c)}} \text{ (eq. 1.35)}$$

Toggling from One Mode to the Other Now that we derived the equations for both CCM and DCM, we need to find a proper way of linking them together. The final device will therefore authorize simulations in both modes with an automatic transition between them. However, we must write the Ga, Gb, and Gc equations to cope with the transition. That is to say, in CCM they should match (1.25 – 1.27). In DCM, on the other hand, they should agree with (1.31 – 1.33). From Figure 1-7e, we can write that

$$\overline{Ipk} = \frac{\overline{V(a,b)} \cdot VD_{ON}}{L} \cdot Tsw \text{ (eq. 1.36)}$$

Combining (1.36) and (1.31) leads to

$$\overline{I_L} = \frac{\overline{V(a,b)} \cdot VD_{ON}}{2 \cdot L \cdot Fsw} \cdot [VD_{ON} + VD_{OFF}] \text{ (eq. 1.37) Solving for } D_{OFF},$$

$D_{OFF} = \frac{2 \cdot \overline{I_L} \cdot L \cdot Fsw}{\overline{V(a,b)} \cdot VD_{ON}} - VD_{ON}$ (eq. 1.38), which corresponds to DCM wheras, for CCM, we have equation (1.28). Equation (1.38) transforms into (1.28) when $2 \cdot \overline{I_L} \cdot L \cdot Fsw = \overline{V(a,b)} \cdot VD_{ON}$ which simplifies to $\overline{I_L} = \frac{Ipk}{2}$ we are in borderline conduction, entering CCM.

Therefore, if we clamp the VD_{OFF} source given by equation (1.38) between (1-VD_{ON}) and zero (or a few mV to avoid possible divide-by-zero errors), we cover both CCM and DCM cases. The final step lies in the generic Ga, Gb, and Gc SPICE expressions allowing both modes to run

$$Ga = I(L) \text{ (eq. 1.39)}$$

$$Gb = \frac{VD_{ON}}{VD_{ON} + VD_{OFF}} \cdot I(L) \text{ (eq. 1.40)}$$

$$Gc = \frac{VD_{OFF}}{VD_{ON} + VD_{OFF}} \cdot I(L) \text{ (eq. 1.41)}$$

$$V_L = V(a,b) \cdot VD_{ON} + V(a,c) \cdot VD_{OFF} \text{ (eq. 1.42)}$$

$$VD_{OFF} = \underbrace{\frac{2 \cdot I_L \cdot L \cdot Fsw}{V(a,b) \cdot VD_{ON}} - VD_{ON} \text{ (eq. 1.43)}}_{DCM \text{ mode}} \text{ or } \underbrace{VD_{OFF} = 1 - VD_{ON} \text{ (eq. 1.44)}}_{CCM \text{ mode}}$$

Where I_L represents the current flowing through the inductor forced by E_L. Fsw is the constant switching frequency (a parameter you will need to feed the model with, as well as the inductor value).

The Final Generic Switched Inductance Model If you now assemble the previous equations into an electrical schematic, you obtain the GSIM model as shown on Figure 1-8a.

This model is not totally complete since the VD_{OFF} clamping circuit is not represented. We purposely put it in Figure 1-8b to detail its operation. As we have explained, we need to clamp the OFF time generator to either (1-D_{ON}) or zero (a bit more to avoid convergence errors). There are several ways to implement this function:

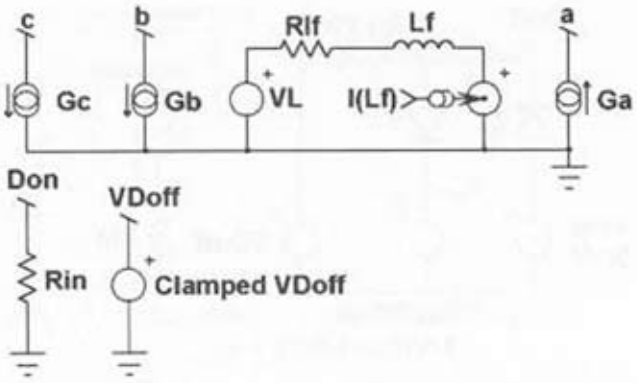


Figure 1-8a
The GSIM model gathers the combined CCM/DCM sources and the inductor current generator.

1. BClampedOFF 1 2 $V = V(VD_{OFF}) > (1-V(D_{ON})) ? (1-V(D_{ON})) : V(D_{OFF}) < 1mV ? 1mV : V(D_{OFF})$

   This expression can be translated this way:

   ```
   IF the voltage of the OFF generator is greater than (1-VDon)
   THEN the voltage delivered by BClampedOFF is 1-VDon)
   ELSE
   IF the voltage of the OFF generator is smaller than 1mV THEN the
   voltage delivered by BClampedOFF is 1mV
   ELSE if neither the above conditions are met THEN deliver the
   voltage of the OFF generator
   ```

2. If this expression fits nicely into one single line, it has the drawback of not being easily portable to other platforms. We prefer the implementation of individual elements to clamp the VD_{OFF} generator, as Figure 1-8b portrays.

Experience also shows that this circuit offers stronger convergence performance than the in-line equation.

The GSIM circuit ensures a full compatibility with DC point calculations and TRANsient runs. The pleasant thing lies in the fact that SPICE automatically performs the linearization for us, therefore allowing AC sweeps in a second.

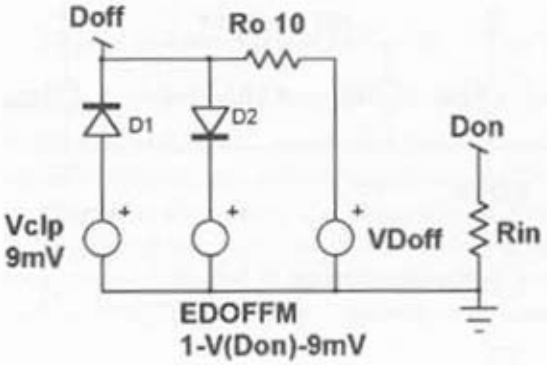


Figure 1-8b
This circuit clamps V(D$_{off}$) between a few mV up to 1-V(D$_{on}$).

Current Mode Models

Numerous *Current Mode Control* (CMC) models have been developed over the past decade. First models suffered from their inability to predict the instabilities inherent to this kind of control. For instance, they were able to properly model the low-frequency response of the CMC power stage, but the current-loop instability had to be addressed as a separate issue. In 1990, Raymond Ridley of VPEC, showed that a CMC power stage was best modeled by a third-order polynomial form [10]. In his thesis, Ridley identified the current sampling action as being the culprit of experimentally observed $F_{switching}/2$ subharmonic oscillations. A CMC actually differs from a voltage mode converter in the way the duty-cycle is generated. In Figure 1-9a-c, Fm describes the "duty-cycle factory," or the electrical way to elaborate it.

In Figure 1-9a the naturally sampled duty-cycle modulator is fed by an error voltage Vc and a reference sawtooth. This is a classical *voltage mode* (VM) *naturally sampled* PWM generator whose small-signal gain is $\frac{1}{Vsaw}$. Figure 1-9b depicts a current mode modulator where the current sense information is added, resulting in a different transfer function Fm for the Pulse Width Modulator section. Since the power stage was not affected by this change, Ridley built his model using the average PWM switch model, to which he added an internal current sampling loop. The new model is presented in Figure 1-9c for steady-state on/off inductor voltages. He(s) is the second-order polynomial form Ridley found to represent the sampling process in continuous time, Ri scales the current information (delivered by

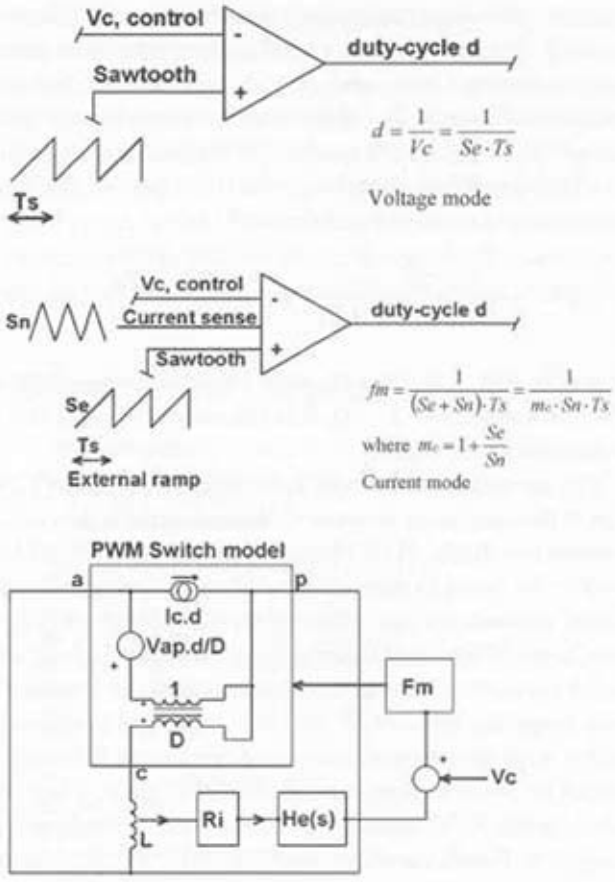


Figure 1-9a, Figure 1-9b, Figure 1-9c
A current-mode supply differs from a voltage-mode supply in the way the duty-cycle is elaborated: S_e is the external ramp slope. S_n is the inductor on-time slope: $Mc = 1.5$ corresponds to 50% ramp compensation.

a simple sensing resistor or via a transformer), and Fm models the duty-cycle generation, as explained in Figures 1-9a (Ri = 0) or 1-9b (Ri ≠ 0). Ridley's model is universal because reducing Ri to 0 shadows the internal current loop and turns the model into voltage mode.

Current Mode Instabilities

A current mode controlled SMPS exhibits one low-frequency pole, ω_p, and two poles that are located at Fsw/2. These poles move in relation to the duty cycle and the external compensation ramp, when present. As you can

imagine, this equivalent second-order filter is affected by a quality coefficient Q. This coefficient, and thus the resulting peaking, depends on the compensating ramp and the duty cycle. Ridley demonstrated that Q becomes infinite at D = 0.5 with no external ramp. It confirms the inherent instability of a current mode SMPS operating at a duty cycle greater than 0.5. The Q coefficient and ω_p, which are part of the $V_{out}/V_{control}$ transfer function, can be expressed as follows:

$$Q = \frac{1}{\pi \cdot (mc \cdot D' - 0.5)} \quad \omega_p = \frac{1}{CR} + \frac{Ts}{LC} \cdot (mc \cdot D' - 0.5) \text{ (eq. 1.45)}$$

where $m_c = 1 + S_e / S_n \cdot S_e$ is the external ramp slope and S_n is the inductor on-time slope. D' = 1 − D, R is the output load, C the output capacitor, and L the main inductor.

The presence of two high-frequency poles in the V_o/V_c transfer function is due to the sampling process of the inductance current. Actually, this process creates two Right Half-Plane zeroes in the current loop that are responsible for the boost in gain at Fsw/2 but also stress the phase lag at this point (these zeroes turn into poles when the voltage loop finally includes the current loop). If the gain margin is too low at this frequency, any perturbation in the current will make the system unstable because both voltage and current loops are embedded. You can fight the problem by providing the converter with an external compensation ramp. This will oppose the duty cycle action by lowering the current-loop DC gain, which will damp the high Q poles in the V_o/V_c transfer function, correspondingly increasing the phase margin at Fsw/2. As other benefits of ramp compensation, Ridley confirmed that an external ramp whose slope is equal to 50 percent (m_c = 1.5) of the inductor downslope could nullify the audio susceptibility in a BUCK converter, as already calculated by Holland [11]. As more external ramp is added, the low-frequency pole ω_p moves to higher frequencies while the double pole will be split into two distinct poles. The first one will move towards lower frequencies until it joins and combines with the first low-frequency pole at ω_p. At this point, the converter behaves as if it is operating in voltage mode. This particular behavior is described in the BUCK simulation section.

Small-Signal Current-Mode Models

If Ridley's models perfectly predict the Fsw/2 oscillations, they were originally written in SPICE2 and were not easy to implement. Thanks to the recent parameter-passing features and definition keywords, the SPICE3

models proposed in this book are really easy to use. One drawback is that they are AC models only and cannot toggle between CCM or DCM. You select the model according to your operating mode. Fortunately, in-line equations automatically calculate all the DC values, for example, the operating duty-cycle for the desired V_{out} at V_{in}. You just need to pass the constant numbers such as inductor value, switching frequency, and so on. Another good point is that Ridley's models are universal: If R_{sense} or R_i has a finite nonnull value, you are in current-mode. If you decrease R_i to zero, you operate in voltage mode. The models are listed thereafter, in PSpice syntax:

Continuous Conduction Mode

```
.SUBCKT PWMCCM 1 2 3 4 5 PARAMS: RI=0.33 L=37.5U FS=50K RL=1 D=0.45
VAP=11 VAC=6 IC=0.8 VP=2
* A P C C'Control
.PARAM TS = {1/FS}
.PARAM PI = 3.14159
.PARAM KF={-(D*TS*RI/L)*(1-D/2)}
.PARAM KR={((1-D)^2*TS*RI)/(2*L)}
**** PWM Switch model ****
E2 7 1 VALUE = { V(17)*(VAP/D) }
G1 1 2 VALUE = { V(17)*IC }
Gxf 7 2 VALUE = { I(Vxf)*D }
Exf 9 2 VALUE = { V(7,2)*D }
Vxf 9 3 0
Rvc 5 0 10MEG
**** He(s) Circuit ****
Hi 10 0 Vxf 1
C1 10 12 {TS/PI}
L1 12 13 {TS/PI}
C2 13 14 {TS/PI}
Re 14 15 =1.57
E1 15 0 12 0 =1E6
R2 12 0 10MEG
**** Summing gains ****
Ed 16 0 VALUE = { V(1,4)*KF + V(4,2)*KR + V(15)*RI + V(5) }
Rd 16 0 10MEG
**** Modulator Gain ****
Efm 17 0 VALUE = { V(16)*1/(VP+(VAC*TS*RI/L)) }
RFm 17 0 10MEG
.ENDS PWMCCM
```

Discontinuous Conduction Mode

```
.SUBCKT PWMDCM 1 2 3 4 5 PARAMS: RI=0.33 L=37.5U FS=50K
+RL=1 D=0.45 VAP=11 VAC=6 VCP=5 IC=0.8 IA=0.16 IP=0.64 VP=2V
* A P C C'Control
.PARAM TS = {1/FS}
.PARAM KF = {-(D*TS*RI/L)}
**** PWM Switch Model ****
```

```
Ri 1 3 { VAC/IA }
Gdi 1 3 VALUE = { V(17)*2*IA/D }
Gf 2 3 VALUE = { V(1,3)*2*IP/VAC }
Gdo 2 3 VALUE = { V(17)*2*IP/D }
Ro 2 3 { VCP/IP }
Rvc 5 0 10MEG
**** Summing Gains ****
Ed 16 0 VALUE = { V(1,4)*KF + V(5) }
Rd 16 0 10MEG
**** Modulator Gain ****
Efm 17 0 VALUE = { V(16)*1/(VP+(VAC*TS*RI/L)) }
RFm 17 0 10MEG
.ENDS PWMDCM
```

Do not be disturbed by the apparent complexity. As we will later discover, all you need to pass are the schematic elements you already know.

GSIM Models and Peak Current Mode

As Ridley showed, the type of supply structure (VM or CM) only affects the duty-cycle generation, not the output stage. The statement remains valid with the GSIM model: We simply need to modify the D_{ON} and D_{OFF} generator to account for peak current mode. In voltage mode, the level you inject inside the model corresponds to D_{ON} (remember, 1V = 100%), whereas D_{OFF} is recalculated depending upon the mode DCM or CCM. In current mode, it slightly differs because the error voltage (the level you inject into the model) defines the peak current setpoint, which according to the A/µs imposed by the inductor, later imposes the final ON time. To evaluate this later parameter, the CM GSIM model makes use of an equation derived by Middlebrook [12]:

$$VD_{ON} = \frac{Verror - \overline{I_L} \cdot K}{Tsw \cdot \left(mc + \frac{0.5 \cdot K \cdot \overline{V(c,a)}}{L} \right)} \quad \text{(eq. 1.46)}$$

where:

K = current loop gain, actually the value of the sense resistor

Mc = slope compensation in V/s

Tsw = switching period

L = inductance of main inductor

$\overline{I_L}$ = averaged inductor current

As in Ridley models, setting K to zero turns the converter into voltage mode (we, however, recommend the use of the appropriate voltage-mode model for these dedicated simulations). The VD_{OFF} generator does not change from the previous CCM and DCM definitions. Please note that GSIM models do not predict Fsw/2 instabilities.

In order to avoid the overabundance of netlists, we will not describe the complete current-mode model but rather discuss it later on in the different converter sections.

Minimum Schematic for Average Simulation

Now that we finished our introduction describing how the models were born, it is time to really put SPICE at work. The very minimum schematic for simulating a converter requires the model (for example, a BOOST, FLYBACK, etc.), the load, eventually a transformer, and an input voltage. Figure 1-10a describes how to put these elements together for a FLYBACK converter.

As you can see, the model features an input whose level controls the duty-cycle (DON in Figure 1-10a). Most of the time, this input directly corresponds to the real duty-cycle you want to impose: 1V = 100%, 652mV = 65.2%, and so on. It is thus advised to externally clamp the circuitry that drives this input between 0 and 1V; otherwise, you will observe wrong results. The duty-cycle source in this example, features two parameters: a DC level leading to the desired operating point, e.g., 22V/10A at a 120VDC

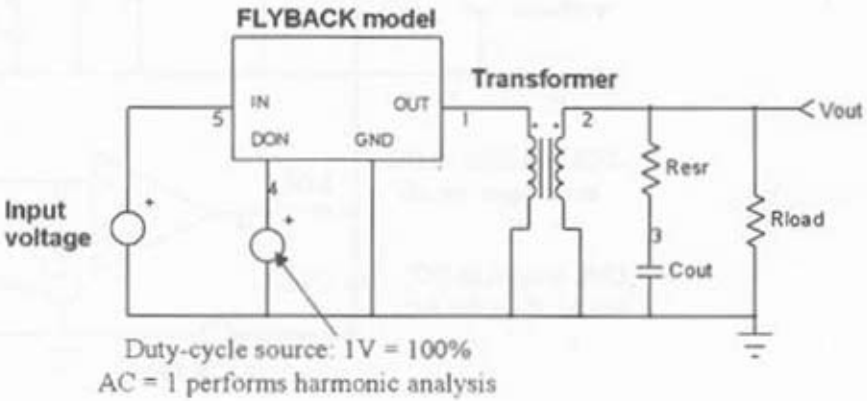


Figure 1-10a
The simplest SMPS SPICE simulation structure (here a FLYBACK converter).

input voltage and a sinusoidal stimulus superimposed over this DC level. In SPICE, this will be written as

```
Vduty nodeA nodeB DC=450mV AC=1V
```

If the external conditions change but you want to keep the same output level, you will need to manually tweak the DC level to stay at the 22V/10A situation, exactly as the feedback loop would do. When there are many iterations to perform, this is not very convenient.

- *Always* look at the output file (.OUT extension) that SPICE generated in order to be sure of the DC point calculation. Cases can arise where the curves look fine, but a wrong operating point makes them false!

Closed and Open-Loop Measurements

A simple method exists that enables you to close the feedback path in DC but open it in AC. If the feedback path is closed in DC, you can adjust the external values at any level within the regulation range (the load, the input voltage, the ESRs, and so on), and the duty-cycle will automatically take the right value to keep the good operating point. Thanks to a simple trick, we

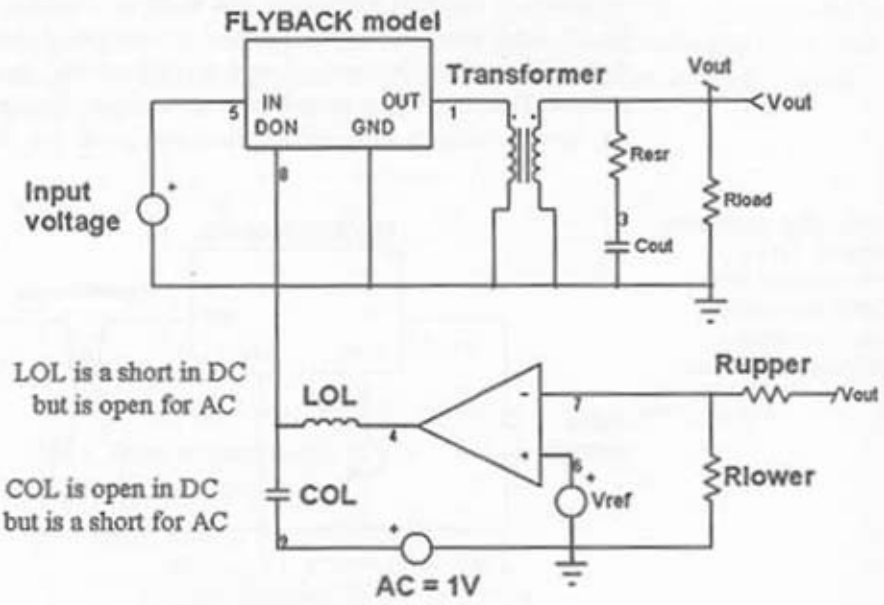


Figure 1-10b COL and LOL effectively open the loop in AC but keep the good DC point.

can disconnect the loop in AC, thus authorizing true open-loop Bode plot generation but still shorting it in DC for the good operating point. Figure 1-10b depicts this old SPICE trick:

If the coil is large enough (for example, 1kH), it will block the error amplifier outcoming wave but will pass its static DC level (remember that SPICE opens all capacitors and shorts all inductors during the DC point calculations). It is then easy to introduce the AC modulation through a 1kF capacitor (a real AC short-circuit) and draw the Bode plot once the simulation completes.

- Sometimes SPICE will fail to converge or will generate strange, noisy plots in AC using these large inductor values. To circumvent the problem, simply add a small 100mΩ resistor in series with LOL.

In Figure 1-10b example, the error amplifier does not feature any compensation network for the sake of clarity. You can, of course, add any of these networks without questioning the trick's validity.

Another possibility consists in including the AC source alone in series with the output of the error amplifier, as shown by Figure 1-10c (please note Vstim source polarity).

By adding proper labels (V_{in} and V_{out}) some graphic processors like Scope5 will immediately display the Bode plot diagram.

- Be sure to inject/observe same quantities: you inject voltage then you observe voltage (for example, V_{out} or V_{err}). This no longer works for shunt regulators where you shall inject current to modify the duty-cycle and finally observe V_{out}.

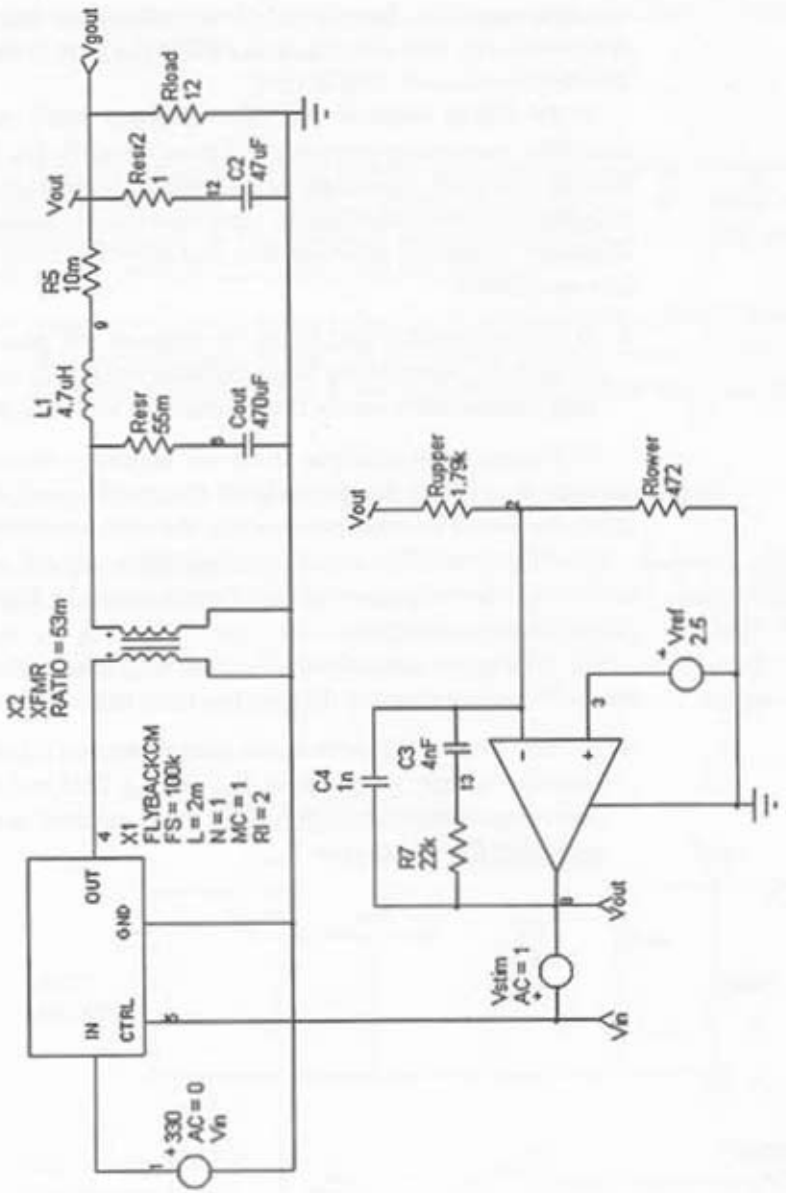


Figure 1-10c
Including the stimulus source in series with the signal is also an option.

CHAPTER 2

Generic Models for Faster Simulations

Generic models are useful when a) you do not need the real component complexity because only first-order effects are of interest and b) you do not have the model and need to create an electrical equivalent one.

Operational Amplifiers

The Simplest Model

Unless you really need to simulate the true *operational amplifier* (OPAMP) for your circuit implements (including offset voltages, bias currents, slew-rates, and so on), simple generic models are usually sufficient to highlight first-order effects. They simulate fast and, by feeding them with numbers, you make them fit your actual OPAMP specs. Figure 2-1a and 2-1b describe how to build very simple devices.

Figure 2-1a is attractive because of the few elements it implies. However, we would recommend its implementation where AC sweeps only are being used (for example, with Ridley models). Why this? Simply because of the lack of output clamping levels that could cause convergence problems when the OPAMP is pushed into its upper or lower stops: $V_{out} = [V(+) - V(-)] \times 1000$. Inserting an active limiter after node 1 works okay (at the node

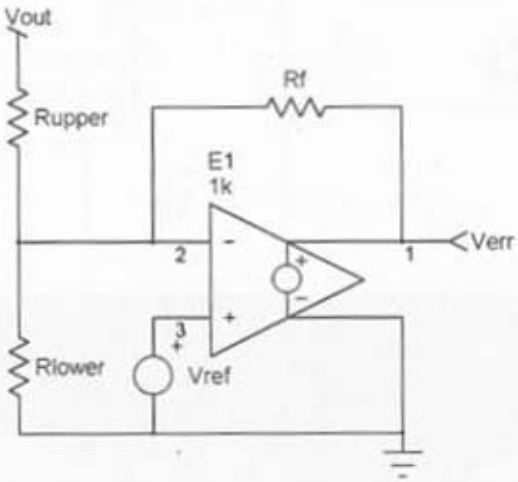


Figure 2-1a
This voltage-controlled voltage source is a possible solution.

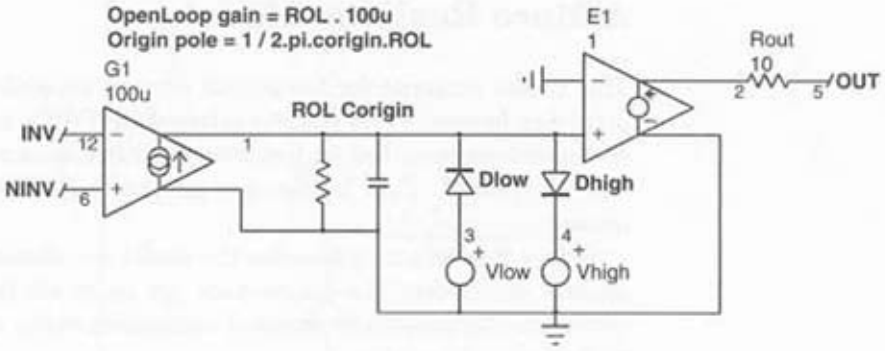


Figure 2-1b
A better option uses a transconductance amplifier and two clamping diodes.

where Rf and E1 connect together), but not directly at E1's output while connecting Rf at the limiter's output: you would run into convergence troubles when the OPAMP starts to clamp.

If clamping represents a real concern, then Figure 2-1b's example offers a better structure by combining a transconductance amplifier and two clamping diodes. If you edit the diode emission coefficient N and set it to 0.01, then you obtain a perfect diode with a null Vf. By tweaking the Vclamp in series with these perfect diodes, you select the lowest and highest output levels of your generic OPAMP. Because you only clamp a few hundred of µA through these elements, it does not bother the simulator. Difficult to do simpler, no? The open-loop gain is set by adjusting the gm of the voltage-controlled current source and the ROL resistor: with an arbitrary 100 µmhos transconductance value, then a 10Meg resistor gives a 60dB open-loop gain. Finally, tail the Corigin capacitor to position the origin pole. If the upper and lower clamping levels are not very precise, they surely are good enough for the vast majority of cases. Following is the Figure 2-1b IsSpice corresponding netlist:

```
.SUBCKT AMPSIMP 1 5 7 {POLE=30 GAIN=30000 VHIGH=4V VLOW=100mV}
* +-OUT
G1 0 4 1 5 100u
R1 4 0 {GAIN/100u}
C1 4 0 {1/(6.28*(GAIN/100u)*POLE)}
E1 2 0 4 0 1
Ro 2 7 10
Vlow 3 0 DC={VLOW}
Vhigh 8 0 DC={VHIGH}
Dlow 3 4 DCLP
Dhigh 4 8 DCLP
.MODEL DCLP D N=0.01
.ENDS
```

A More Realistic Model

This model accounts for the output current capability of the operational amplifier. In most PWM ICs, the internal OPAMP is an open-collector type: it can sink current, but its limitation in current-source allows the user to easily bypass it. That is the case for the UC384X controller family, for instance.

Figure 2-1c and 2-1d describe the model we adopted in all the following generic subcircuits. The parameters you enter via the schematic capture automatically adjust the internal component value to shape the OPAMP performance as needed.

Sources with a Given Fan-Out

Some applications, such as internal voltage reference, cannot always be modeled as a simple source in series with a static resistor. Another important parameter is the fan-out or the maximum output current the source can supply before giving up. The simplest way is to describe this behavior using a single in-line equation. If the reference level is made dependent of the input node (imagine the reference block is supplied from a Vcc line), we naturally describe its DC audio susceptibility (also called line ripple rejection).

Suppose that we create a 5V source affected by a normal dynamic impedance Rout of 2.5Ω and a positive line ripple rejection of 60dB. If our output current is less than a given value (1.5mA in this example), the output level is not affected, except by the normal Rout loss. The in-line equation, or the Analog Behavioral Modeling (ABM) description could look like:

B1 INT GND V=Iout<1.5mA ? (Vref+Vref*1m)

IF the output current is less than 1.5mA **THEN** the source delivers [(Vref + Vref * 1m)] in series with a 2.5Ω resistor.

Now, we need to define how the output voltage decreases, or what resistive slope R_{slope} affects the output in overcurrent condition. If we select a 10kΩ slope, the final equation looks like:

B1 INT GND V=Iout<1.5mA ?
(Vref+Vref*1m):(Vref+Vref*1m)−10k*Iout+15

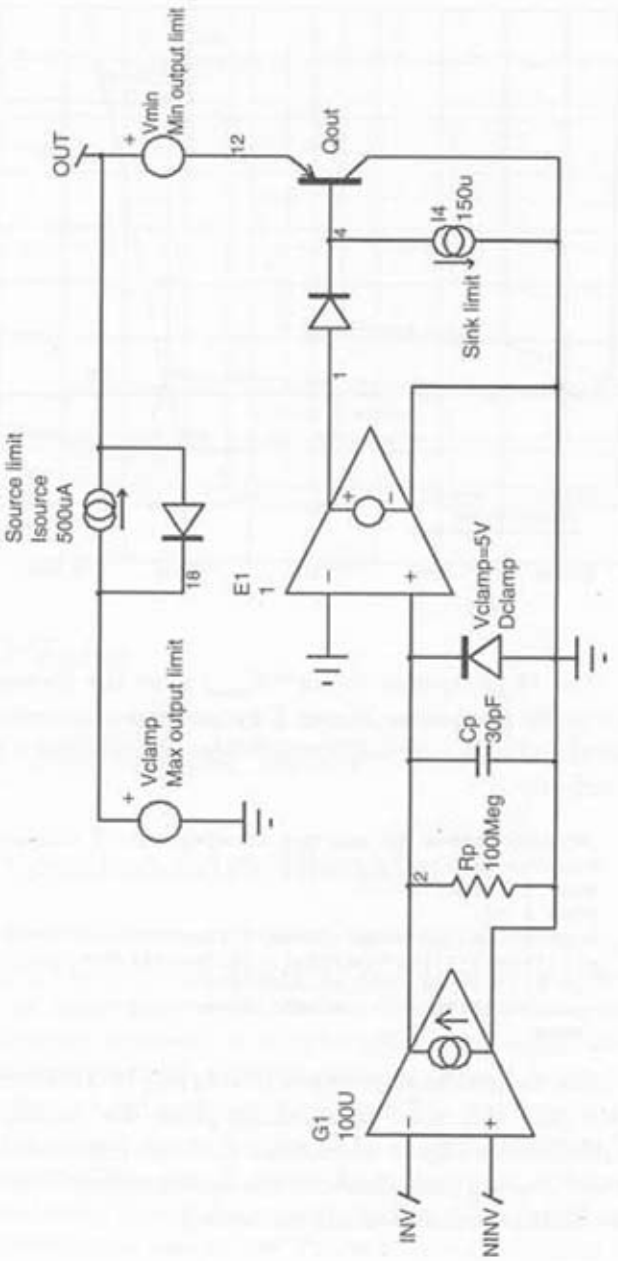


Figure 2-1c
A more realistic OPAMP with given sink/source capabilities.

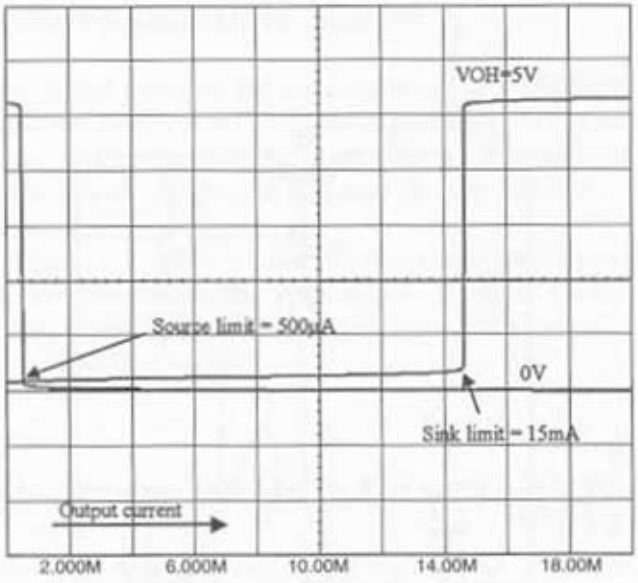


Figure 2-1d
A more realistic OPAMP with given sink/source capabilities.

The 15 parameter (Imax * R_{slope}) gives the necessary offset to properly shape the final curve. Figure 2-2 shows how the model finally behaves when using the following description where the parameter-passing feature brings flexibility:

```
.SUBCKT REFVAR In Out Gnd (Vref=5 Zo=2.5 Slope=10k Imax=1.5m
Ripple=-1mV)
Rout 5 6 {Zo}
vdum 6 Out
Bout 5 Gnd V=I(Vdum)<{Imax}?(({Vref}-V(in)*{Ripple}):
+((({Vref}-V(in)*{Ripple})-{Slope}*I(Vdum))+({Slope}*{Imax}))
+>0 ? ((({Vref}-V(in)*{Ripple}))-
+{Slope}*I(Vdum))+({Slope}*{Imax})):0
.ENDS
```

The netlist example shows how to mix IF-THEN-ELSE expressions into one line. You need to carefully place the parenthesis, especially with CADENCE's PSpice when more than one expression shares the same line. The following lines illustrate the syntax difference for a given expression in which three conditions are embedded:

IsSpice

```
B1 15 0 V=ABS(V(1,3))>{VTHRES) ? 100V : ABS(I(VDUM))>{ISUS) ? 100V:
+ABS(V(1,3))>V14)?100V:V(19)>3V ? 100V : 10N
```

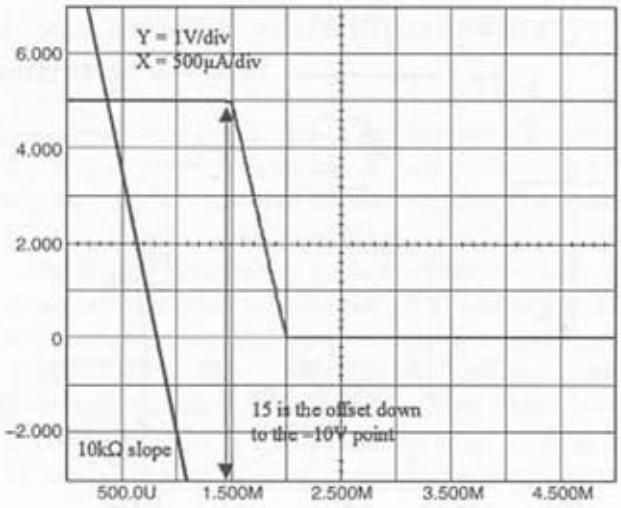


Figure 2-2
Without the offset, the output would immediately dip at 5V-(10kΩ . 1.5mA) and a discontinuity would appear.

PSpice

```
E1 15 0 VALUE={ IF ( ABS(V(1,3))>{VTHRES}, 100V, IF
( ABS(I(VDUM))>{ISUS}, 100V, IF ( ABS(V(1,3))>V(14), + 100V, IF
( V(19)>3V, 100V, 10N )))) }
```

Leading-Edge Blanking

Every time the main switch closes and discharges parasitic capacitors (or stops a conducting diode in CCM converters), a current spike takes place in the semiconductor. Depending on the conditions, this spike can cheat the current limit section or the reset comparator in current-mode structures. An adequate RC network cures the default, but most of today's ICs implement a Leading Edge Blanking (LEB) circuitry. It consists in transmitting the sensed current pulse only a few hundred nanoseconds after it has started. That way, if a very big spike occurs at the switch closing, the LEB naturally blinds the system for the given period and fully transmits the information afterwards. Figure 2-3a shows how to simply connect a delay line together with a comparator in order to build an efficient LEB. Figure 2-3b details the final behavior.

By feeding the delay line subcircuit with a given transfer time, you tailor the LEB at your convenience.

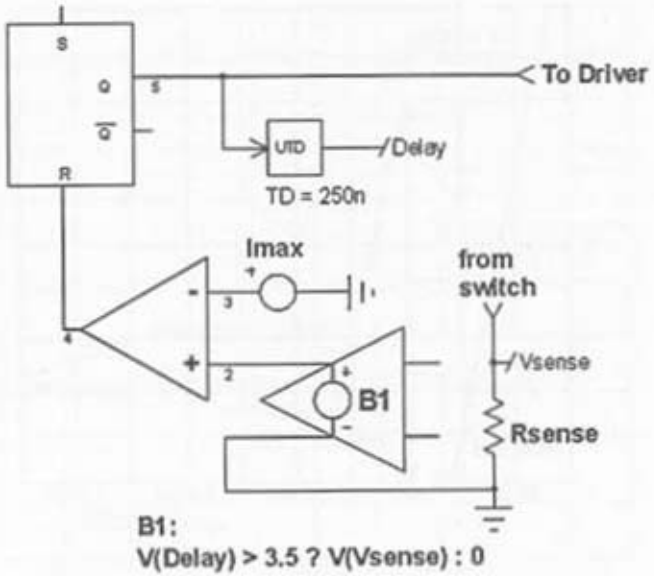


Figure 2-3a
B1 blanks the sense information until Delay goes high.

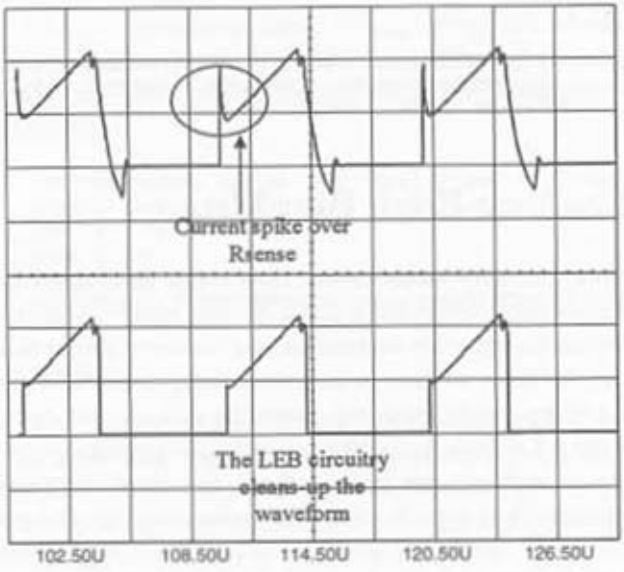


Figure 2-3b
The lower trace clearly shows the 250ns LEB action.

Comparator with Hysteresis

Analogue designers rarely leave a fast comparator without introducing a bit of hysteresis. This feature strengthens the noise immunity and ensures clean and sharp transitions. If adding resistors across the comparator allows a quick hysteresis implementation, the method requires a bit of calculation to determine the true hysteresis value you finally put.

By dynamically changing the reference voltage according to the output state, you can select the amount of hysteresis you need. Figure 2-4a depicts the parts arrangement to generate such a circuit. When the comparator output is at low state (<3V), then the reference equals 5V. Once the output has toggled to the high state, the reference becomes 3V and forces the input to decrease below this level to come back to the initial state: you created a 2V hysteresis, as demonstrated by Figure 2-4b, for which Vin (V1) was

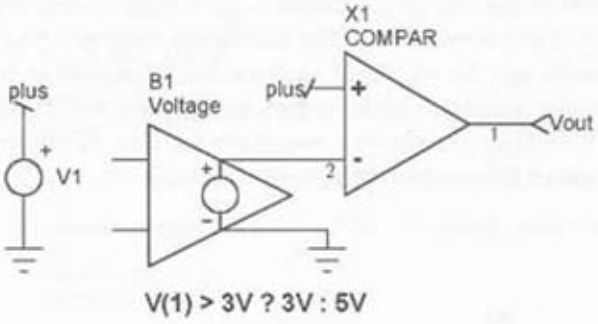


Figure 2-4a
A simple arrangement provides a known amount of hysteresis.

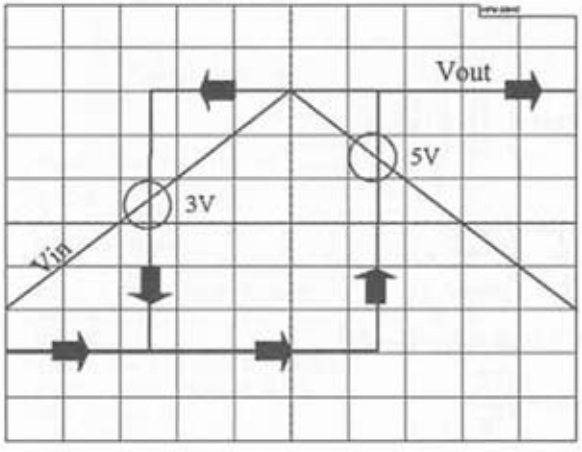


Figure 2-4b
In this example, the system introduces 2V of hysteresis.

ramped up and down again. A typical convergence error occurs if, by mistake, you reversed the equation conditions.

Transformers

To model a simple dual-winding transformer, we can use the SPICE primitive *k*, which describes the coupling ratio between a primary and a secondary. Figure 2-5a shows how to place the inductors around this coupling element. However, as simple as this can be, you do not gain much insight into the transformer elements: you have to derive the leakage inductor value from k and the turn ratio as well. It can sometimes be unclear and painful when iterations are needed (for example, adjust the leakage to assess the effect of a clamping network).

A better solution lies in using an electronic transformer as depicted by Figure 2-5b. This device models a theoretical transformer of infinite bandwidth (including DC). Thanks to its simplicity, the corresponding computational time is very small. The ratio is normalized to the primary (for example, Np=20 and Ns=3 would mean a 1:0.15 passed to the model). A negative number simulates an inversion, for example, a FLYBACK application.

Following are the two necessary netlists to implement the Figure 2-5b model in PSpice and IsSpice syntax:

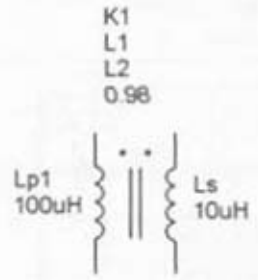


Figure 2-5a
With this structure, you need to derive Lleak manually.

$$k = \sqrt{1 - \frac{Lp_{Sshort}}{Lp_{Sopen}}}$$

$$\Longrightarrow Lleak = Lp \cdot (1 - k^2)$$

$$\Longrightarrow N = \sqrt{\frac{Ls}{Lp}}$$

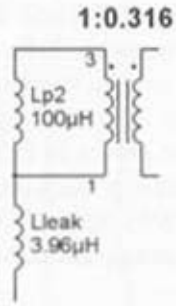


Figure 2-5b
This solution offers immediate insight on the transformer.

⟹ Lleak is immediate

⟹ N is clear

IsSpice

```
.SUBCKT XFMR 1  2  3  4 (RATIO=???)

RP 1 2 1MEG
E 5 4 1 2 (RATIO)
F 1 2 VM (RATIO)
RS 6 3 1U
VM 5 6  VM 5 6
.ENDS
```

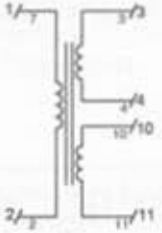
PSpice

```
.SUBCKT XFMR 1 2 3 4 PARAMS:
+RATIO=1
RP 1 2 1MEG
E 5 4 VALUE = { V(1,2)*RATIO }
G 1 2 VALUE = { I(VM)*RATIO }
RS 6 3 1U

.ENDS
```

A dual transformer will simply combine the above equations:

```
.SUBCKT XFMR-AUX 1 2 3 4 10 11 (RATIO_POW=??? RATIO_AUX=???)
*
*RATIO_POW = A
*RATIO_AUX = B
*
```




```
* 1:A
* 1:B
RP 1 2 1MEG
E1 5 4 1 2 {RATIO_POW}
F1 1 2 VM1 {RATIO_POW}
RS1 6 3 1U
VM1 5 6
E2 20 11 2 1 {RATIO_AUX}
F2 2 1 VM2 {RATIO_AUX}
RS2 21 10 1U
VM2 20 21
.ENDS
```

Positive ratios for A and B describe pin 3 and 10 as the positive outputs (for example, for a FORWARD) by respect to 1. By entering negative values for A and B, you simulate separate or both windings in FLYBACK mode.

Floating nodes, as encountered in isolated supplies built with the above transformers, often generate matrix errors in SPICE simulators. To avoid this pitfall, simply add a 100Meg resistor between nodes 4 and 11 and the ground. IsSpice implements .OPTIONS RSHUNT=100Meg, which places a shunt element between each node and ground, thus easing the DC convergence.

Appendix B shows how to measure the physical parameters of your prototype and bring them back into the model. Reference [14] explains in detail how the parameters were derived.

Astable Generator

An astable generator is often needed wherever switching cycles exist. Many methods exist to create a relaxation mechanism. Figure 2-6a proposes a possible solution, while Figure 2-6b displays the simulation results. The upper- and lower-capacitor threshold can be changed by rewriting equation B1.

A Simple Voltage-Controlled Oscillator

A VCO does not differ too much from the Figure 2-6a example. Just replace the fixed current source by either a transconductance amplifier (G state-

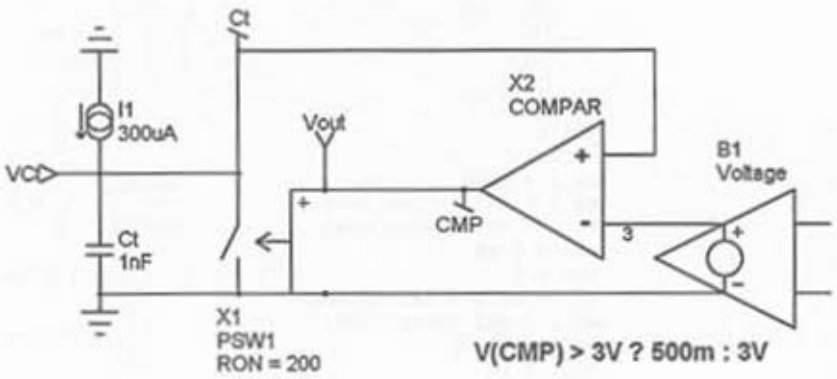


Figure 2-6a
A simple ramp/square wave generator built around one B element, which provides the necessary hysteresis

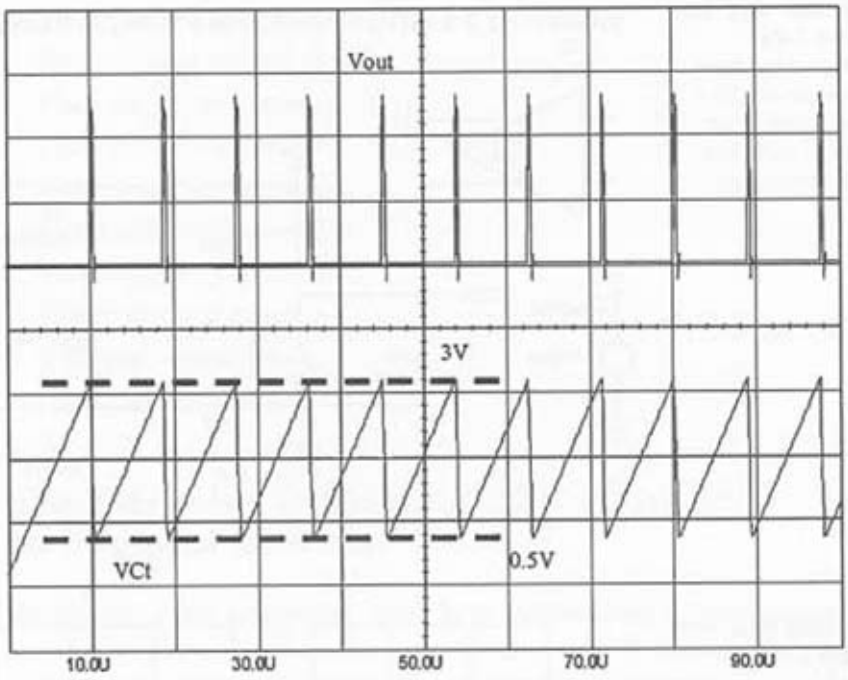


Figure 2-6b
A 300µA together with a 2.5V capacitor dynamic generate a 113kHz pattern.

ment) or a voltage-controlled current generator in a B function. That way, you can easily bound the maximum and minimum frequencies within an input range as shown in Figure 2-7a.

Equation B2 fixes the active input range between 3V and 100mV where the current varies from 350µA down to 10µA. Simulation results are shown in Figure 2-7b.

Complete Generic Controllers

As we said, using a complete PWM model can sometime lead to prohibitive simulation times simply because of the inherent model complexity. There are some situations where you really need this level of detail. For a first-order approach, it is simply an overkill. The following lines describe how to realize generic models that simulate fast and converge well. The library files available on the CD-ROM (extension .LIB) include the following models, declined in PSpice, IsSpice, and Micro-Cap syntax:

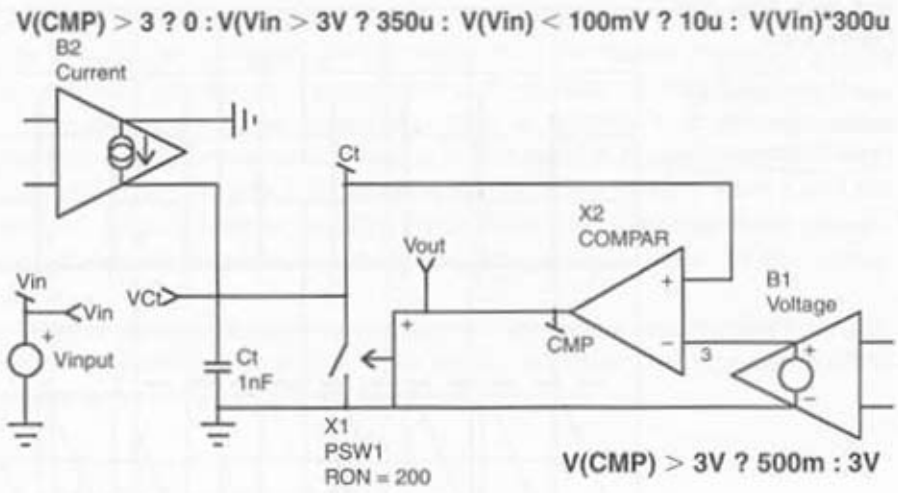


Figure 2-7a
Replacing the fixed current source by a transconductance reveals a complete VCO architecture.

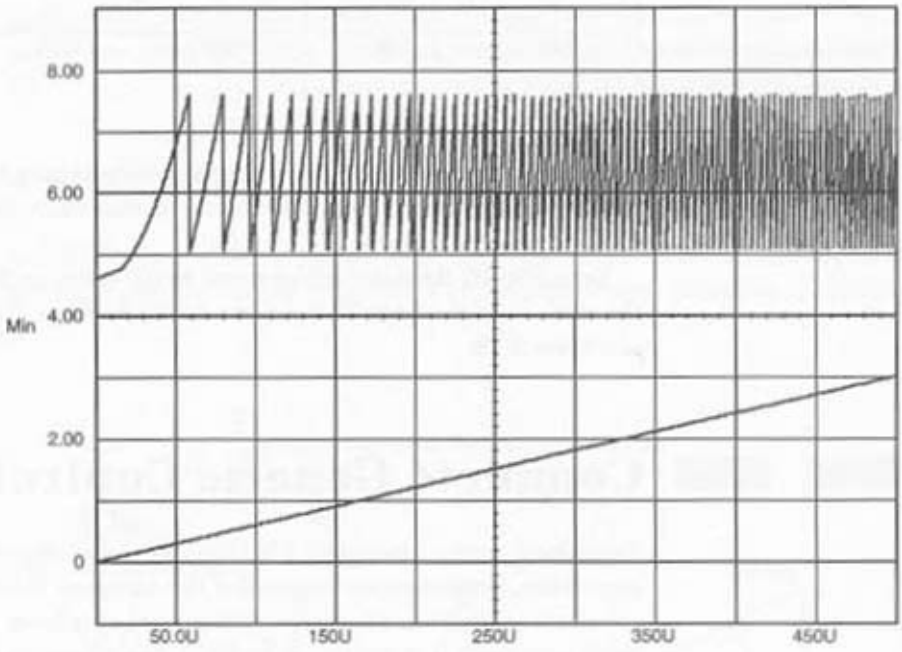


Figure 2-7b
Ramping the input level sweeps the output frequency of our VCO.

Single-output current-mode
Single-output voltage-mode
Push-pull current-mode
Push-pull voltage-mode
Half-bridge current-mode
Half-bridge voltage-mode
Full-bridge current-mode
Full-bridge voltage-mode
2 Switch current-mode
Dead-time generators

The Berkeley B Element, the Standard Behavioral Element

An efficient PWM model that claims to be fast and easy to use must include generic functions. For instance, it would not be clever to model an internal current comparator with the complete transistor architecture of a LM311 or a LM193. Fortunately, there is a simple in-line equation that can describe the perfect comparison function. By adding some passive elements to incorporate various effects (propagation delay, input offset voltage, and so on), we can achieve the functionality we need without sacrificing the simulation speed.

The nonlinear controlled source, or B element, is part of Berkeley SPICE3, which was released to the public domain in 1986. Depending on the compatibility of your SPICE3 simulator, the corresponding syntax may vary significantly. B elements can be linear or nonlinear current or voltage sources. Some vendors have expanded the B element syntax to include BOOLEAN and IF-THEN-ELSE functions. For INTUSOFT's IsSpice and CADENCE's Analog WorkBench Spice Plus (AWB), the writing of I or V math equations using B elements is the same because both are SPICE3 compatible. For example, current/voltage generators whose current depends on various nodes can be expressed as:

```
B1 1 0 I = V(5,8)*100*V(10)/(V(8)+V(12))    ; IsSpice or AWB current
                                              source
B2 2 0 V = V(9,8)*500*V(12)                 ; IsSpice or AWB voltage
                                              source
```

CADENCE PSpice has departed from the Berkeley standard and uses a different syntax. PSpice modifies the standard calls for dependent voltage-

controlled sources (E and G elements). The equivalent PSpice examples are as follows:

```
G1 1 0 VALUE = { V(5,8)*100*V(10)/(V(8)+V(12)) }     ; PSpice
                                                       current
                                                       source
E2 2 0 VALUE = { V(9,8)*500*V(12) }                  ; PSpice voltage
                                                       source
```

Implement Your Logical Operations

As stated in the above paragraph, BOOLEAN and IF-THEN-ELSE expressions have become a part of most vendors' B elements. Their implementation also depends on the SPICE simulator. INTUSOFT exploits the concept of "binary" voltage, that is to say, a node value that is lower or higher than a user-defined threshold can be associated with 1 or 0. This threshold is driven by the keyword LTHRESH, whose value is set via an .OPTIONS line. Two other options, LONE and LZERO, will define the HI and LO electrical values that are delivered by a B element source when it is performing such BOOLEAN operations. A simple NAND equation between two nodes is simply expressed as:

```
BNAND 3 0 V=-( V(1) & V(2) )     ; IsSpice complemented (-) AND
                                   operation between V(1) and V(2)
```

Because the other SPICE simulators do not directly support this syntax, it would be much easier to adopt a simpler expression in order to simplify any further translations. If we pass the logical thresholds directly into the equation, we obtain the following IsSpice IF-THEN-ELSE statement:

```
BNAND 3 0 V= (V(1)>800M) & (V(2)>800M)?   0V :   5V
```

In other words,

```
IF V(1) is greater than 800mV AND V(2) is greater than 800mV, THEN
V(3,0)=0V; ELSE V(3,0)=5V
```

Now the translation to AWB and PSpice syntax is more straightforward:

```
E_BNAND 3 0 VALUE = { IF ( (V(1)>800M) &        ; PSpice NAND gate
(V(2)>800M), 0V, 5V ) }
BNAND 3 0 V = IF ( (V(1)>800M) &&               ; AWB NAND gate
(V(2)>800M), 0, 5 )
```

Note that the AWB parser does NOT accept suffixes for the passed numerical values, and the && symbol is doubled as in the C language to distinguish a logical AND from a binary AND. The diversity in implementing the B elements is only bound by the user's imagination. What we have

shown previously is only a small part of the possibilities offered by Behavioral Modeling via the B element.

If your simulator does not support B element modeling, the situation becomes complex. Some examples on how to model the logical functions with SPICE2 syntax are given at the end of this chapter.

Here's an application example, a simple voltage limiter that limits the differential voltage of nodes 1 and 2 between 100mV and 1V:

```
E1 3 0 TABLE {V(1)-V(2)} 100M, 100M 1,1          ; PSpice
E1 3 0 VALUE = { IF ( V(1,2)<100mV,
+100mV, IF V(1,2)>1, 1, V(1,2) ) ) }              , also PSpice
B1 3 0 V = IF ( V(1,2)<\<>1, IF
+(V(1,2)<\<>100M, 100M, V(1,2)),1)                ; AWB (No suffixes!)
B1 3 0 V = V(1,2)<\<>100MV ? 100M :               ; IsSpice
+V(1,2)>1 ? 1 : V(1,2)
```

In other words,

```
IF V(1,2) is less than 100mV, THEN V(3,0)=100mV; ELSE IF V(1,2) is
greater than 1V, THEN V(3,0)=1V, ELSE V(3,0)=V(1,2)
```

B elements switch in essentially a zero time span. This characteristic may create convergence problems on transitions associated with these perfect sources. We recommend that you tailor the output switching times in a more realistic manner. A simple RC network is suitable for this purpose. A perfect comparator that accounts for these conditions is given in the following paragraph. We have included it in a SUBCIRCUIT in order to highlight the philosophy of constructing your own models:

```
.SUBCKT COMP     1    2    3

*                (+)  (-)  OUT
E1 4 0 VALUE = { IF ( V(1)>V(2), 5V, 0 ) }      ; PSpice syntax
RD 4 3 100                                      ; RC network
CD 3 0 100P                                     ; to slow down
                                                  transitions

.ENDS COMP
```

You need to account for a propagation delay? Add a delay line in series with the output and your netlist becomes:

```
.SUBCKT COMP      1     2     3

*                 (+)   (-)   OUT
E1 4 0 VALUE = { IF ( V(1)>V(2), 5V, 0 ) }
RD 8 3 100
CD 3 0 100P
T1 4 0 8 0 Z0=1 TD=250ns ; tailor TD to your needs, here a 250ns
;example
RL 8 0 1
.ENDS COMP
```

Now that we have reviewed the basics of generating in-line equations, let's dip into the nitty-gritty of a constant frequency CM PWM controller.

Current Mode Controllers, a Well-Known Architecture

The modeling of such a block consists of: a) defining and testing each subcircuit individually, and b) assembling all of these dominolike circuits to form the complete generic model. All individual blocks should be tested before they are used within larger models. Rugged models (in terms of convergence capabilities) are those that work with all the default SPICE options: if you need to relax an option (like ITL1 or RELTOL) to make your prototype model converge, it is not an encouraging sign for the final implementation.

Following are some recommendations that will ease your writing task:

- Draw the symbol of your generic model with your favorite schematic capture tool. Once this is done, you won't have to worry about incorrect pin connections (as you would if you were creating a SPICE netlist with a text editor). Internal subcircuit testing is simplified since you may then access the connection pins directly in the schematic model, and the pin-passing process (from schematic to netlist) is performed automatically.
- Place comments on every pertinent line, either with a "*" in column one (for a complete line), or a ";" immediately preceding a comment within a line. Also, use different commented header names for each section of code within the listing.
- Use descriptive names for the components you assemble in the subcircuit netlist, for example, VCLOCK for a clock source, RDUM for a dummy load, and so on.
- Use subcircuits whenever a function is called more than once. Even if the function is only called once, you can create a subcircuit and therefore simplify the netlist. This will also facilitate the writing of new models because the .SUBCKT functions are easily pasted into the netlist. Also, if required, the conversion process to another platform will be greatly simplified.
- Use realistic parameter values for primitive SPICE components such as the diode (D). These models may generate convergence problems since some of the default parameters are set to zero. For example, .MODEL DMOD D (TT=1N CJO=10P RS=100M).
- Use a main subcircuit pin number of up to 10 or 20 and use incremental decimal digit notation as you change the internal function. This is especially recommended for complex models in which

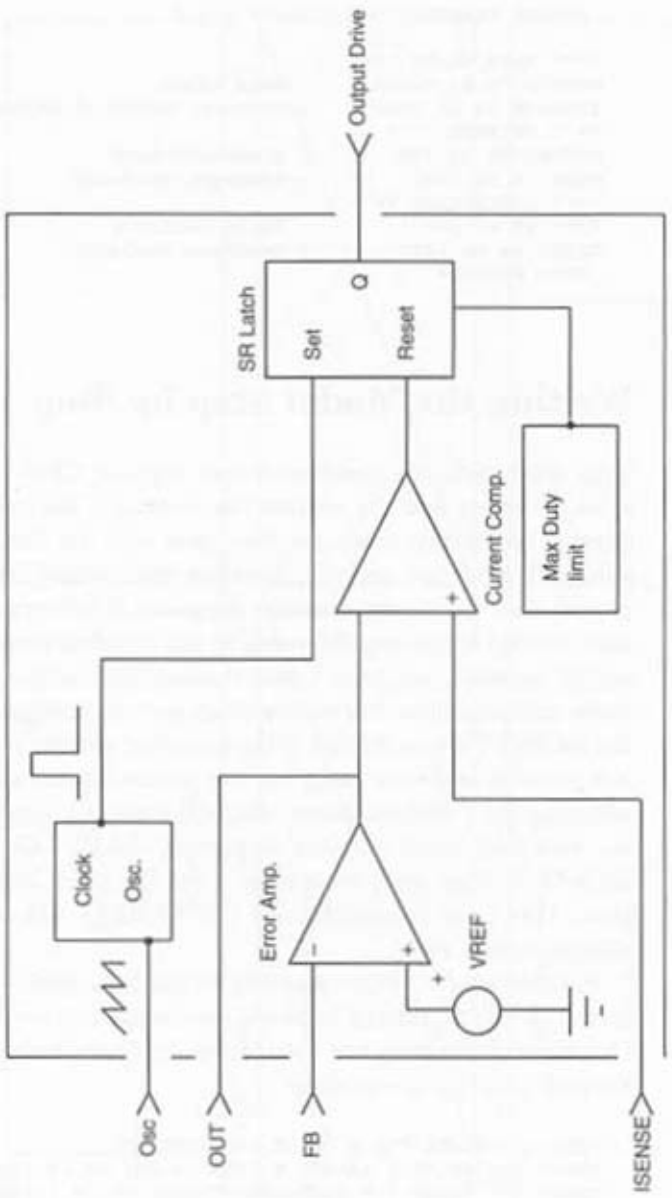


Figure 2-8
The internal structure of a standard single-output current-mode controller.

the parent subcircuit may be large. The following is an arbitrary example, where nodes 7 through 19 are preserved in order to output test signals or add pins:

```
.SUBCKT EXAMPLE          1 2 3 4 5 6

**** MAIN CLOCK ****
VCLOCK 20 21 PULSE       ; Main clock
ICHARGE 22 24 10MA       ; Current charge of capacitor C1
**** TRIGGER ****
RTHRES 30 33 10K         ; Threshold high
CDEL 33 38 10NF          ; Propagation delay
**** COMPARATOR ****
RINP 40 42 10K           ; Input resistor
RFEED 45 49 120K         ; Feedback resistor
.ENDS EXAMPLE
```

Writing the Model Step by Step

Let's start with the synchronization signals, Clock, Osc., and Max. duty cycle. The first one will initiate the on-time of the external switch by triggering the flip-flop latch. Its frequency sets the functioning period of the entire PWM circuit, and will therefore require user input (PERIOD). Osc. is provided for ramp compensation purposes. It delivers a signal that is equivalent to that which was delivered by the classical linear charge of the external RC network oscillator. Using the oscillator ramp is a possible option for ramp compensation, but others exist, such as charging a RC network from the MOSFET driver output. If the capacitor voltage is kept at around 1 volt, it is possible to obtain a very low impedance linear ramp, without adversely affecting the PWM oscillator. Osc. will have the same period as Clock, but the user will select its peak amplitude (RAMP). Once the Clock pulse is issued, the Max. duty cycle must reset the latch after a specific period of time. This time is user-defined (DUTYMAX) and selects the maximum allowable duty cycle.

Parameters for IsSpice and PSpice are quite similar in format. The parameter, or any equations between parameters, is enclosed by curly braces. Our three generators are listed next. Arbitrary node numbers are used to simplify their understanding:

```
VCLK 1 0 PULSE 0 5 0 1N 1N 10N {PERIOD}
VRAMP 2 0 PULSE 0 {RAMP} 0 {PERIOD-2N} 1N 1N {PERIOD}
VDUTY 3 0 PULSE 0 5 {PERIOD*DUTYMAX} 1N 1N {(PERIOD-
+PERIOD*DUTYMAX)-2N} {PERIOD}
```

A quick simulation of this set of equations appears in Figure 2-9, where a maximum duty cycle of 0.5 was selected.

The current comparator requires a simple equation followed by a RC network that slows down its transitions. The model is the same as the one given in the previous example.

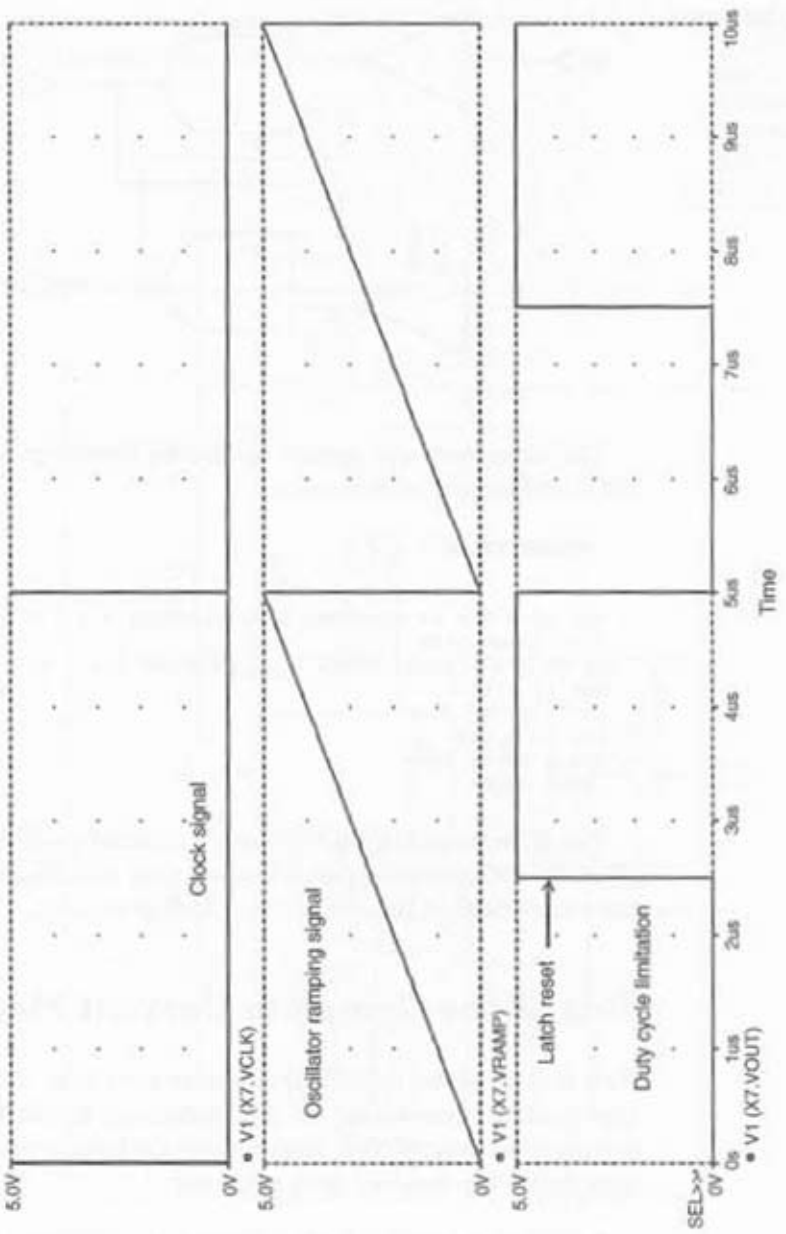


Figure 2-9
PSpice Simulation results of the timing portion of the current-mode model.

The SR latch may be defined in many ways. Again, for straightforward translation, we do not recommend the use of a proprietary flip-flop model. You can draw a classical RS flip-flop and add a couple of inverters in order to generate the required signals. Figure 2-10 shows the electrical circuit.

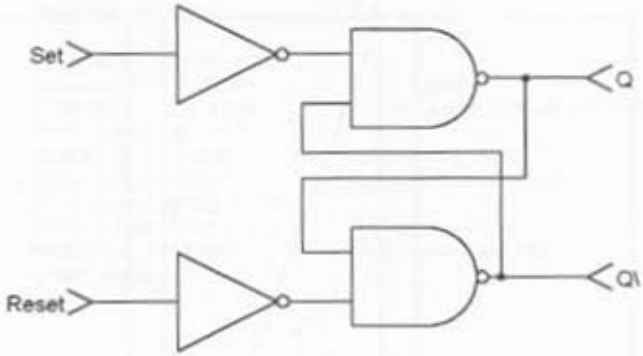


Figure 2-10
A classical RS latch made of standard gates, easier to convert than true proprietary functions

The subcircuit will appear as shown following, according to common AWB and IsSpice syntax rules:

```
.SUBCKT FFLOP 6 8 2 1

*              S R Q Q\
BQB 10 0 V = (V(8)<800M) & (V(2)>800M) ? 0 : 5 ; one input inverted
;two input NAND
BQ 20 0 V = (V(6)<800M) & (V(1)>800M) ? 0 : 5
RD1 10 1 100                                    ;delay elements
CD1 1 0 10p IC=5
RD2 20 2 100
CD2 2 0 10p IC=0
.ENDS FFLOP
```

The IC statements are mandatory to avoid conflicts when SPICE computes the DC operating point. You will then add the keyword UIC (Use Initial Conditions) at the end of the .TRAN statement.

Test of the Complete Current-Mode Model

Now that all of the individual elements have been defined and tested, it is time to place them within the final subcircuit model, PWMCM. The output driver model is simplified, and converts the latch levels to user-defined voltages that are associated with a resistor:

```
E_BOUT 15 0 VALUE = { IF ( V(10)>3.5, {VOUTHI}, {VOUTLO} ) } ; node
;10 is the latch output
ROUT 15 1 {ROUT}
```

The test circuit is a buck converter that delivers 5V at 10A. All of the elements have been calculated using the new release of POWER 4-5-6 [13],

which was developed by RIDLEY Engineering. Figure 2-11a depicts this switch-mode converter:

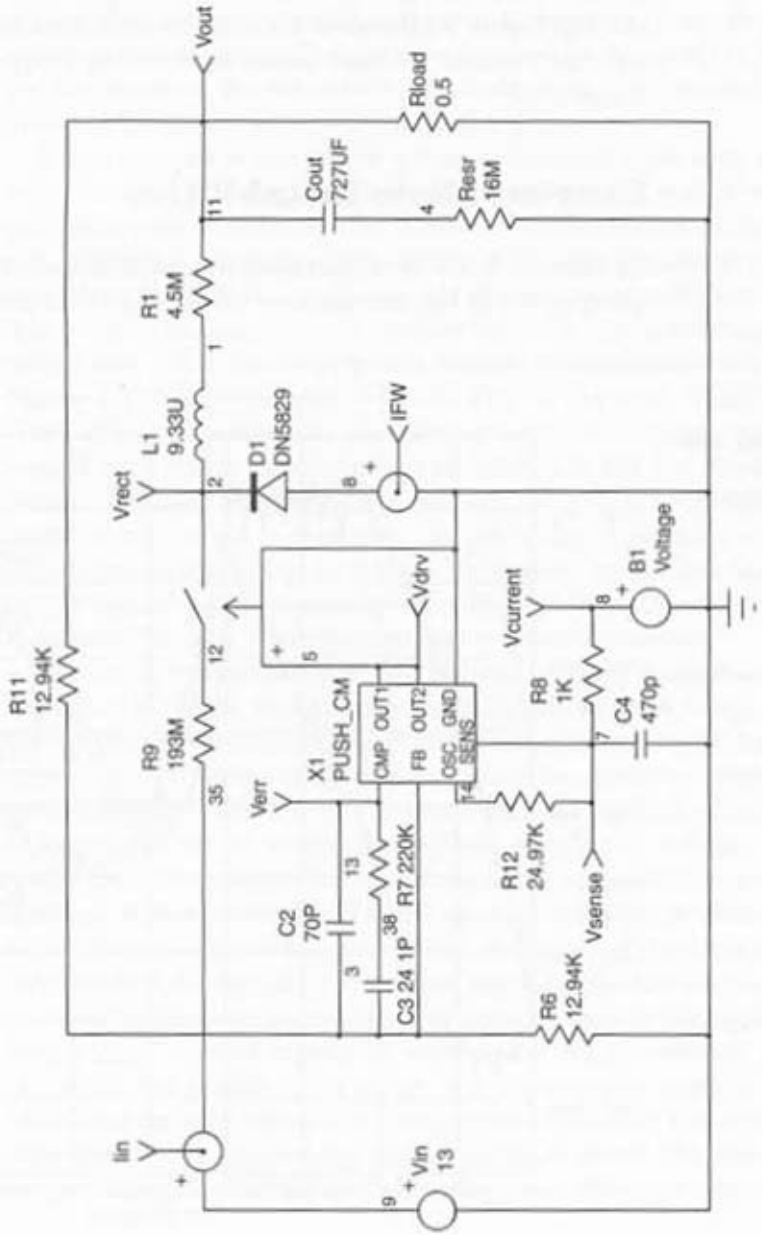


Figure 2-11a
This example demonstrates the ease of implementation for a generic CM model.

The ramp compensation is accomplished by summing a fraction of the oscillator sawtooth and the current sense information. It has several beneficial effects that we will discuss later on. This circuit has been simulated in 50s upon a P350 machine for a 400ms transient run. With this simulation speed, output response to load or input step can be accomplished rather quickly. Figure 2-11b shows the start-up conditions before the output voltage has reached its final value. A switching frequency of 200kHz was selected.

Current Mode Instabilities

In Chapter 1, we have discussed the instabilities introduced by the sampling action in the current loop. To highlight this phenomenon, let's open

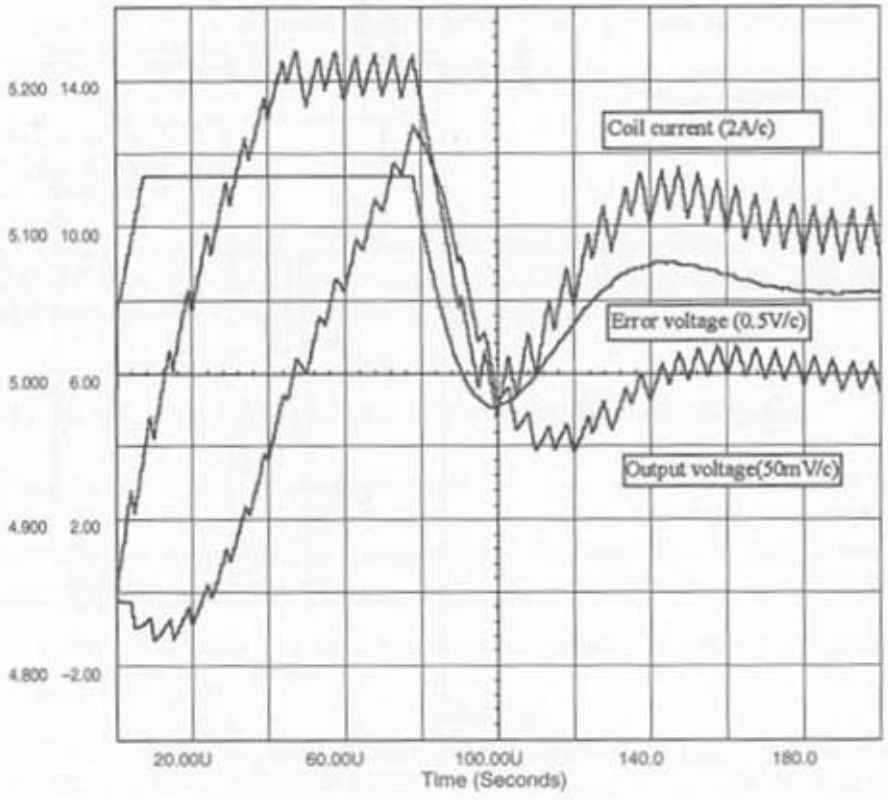


Figure 2-11b
Simulation results of Figure 2-11a example.

the voltage loop of the Figure 2-11a circuit and place a fixed DC source at the right tail of R11 (node 11). R12 is elevated to 1MEG in order to suppress any ramp compensation. If we abruptly change the input voltage from 18V to 12.5V, the Fsw/2 component appears (100kHz) and is damped after several switching periods, since the duty cycle is less than 0.5. Further stressing of the output would lengthen the damping time or produce a steady-state oscillation. The result is depicted in Figure 2-11c, where a filter has removed the main switching component from the coil current to allow the Fsw/2 signal to be properly viewed.

If this network is now closed within a high-gain outer loop, any current perturbation will make the entire system oscillate at Fsw/2, even if the loop gain has a good phase margin at the 0dB crossover frequency. This so-called gain peaking is attributed to the action of the high-Q poles, which push the gain above the 0dB line at Fsw/2, and produce an abrupt drop in phase at this point. If the duty cycle is smaller than 0.5, the oscillations will naturally cease, but if the duty cycle is greater, the oscillation will remain, as Figure 2-11d demonstrates with the FFT of the error amplifier voltage (Vin=11.5V). In conclusion, providing an external ramp is a wise solution, even if your SMPS duty cycle will be limited to 0.5: the Fsw/2 Q will be reduced, thereby preventing oscillations. For FORWARD converters, the magnetizing current is present in the sense signal and adds a slope of the same order of magnitude as the natural current ramp. That is why people do not usually run into trouble with CMC FORWARDs operating at duty-cycle less than 50%, without external compensating ramp.

The audio susceptibility is also affected by slope compensation. Ridley showed in his work that an external ramp whose slope is equal to 50% of the inductor downslope could nullify the audio susceptibility. As previously stated, excessive ramp compensation makes the converter behave as if it is in voltage mode, with a resulting poor audio susceptibility. Also, if minimal compensation or no ramp is provided, good input voltage rejection is achieved and the phase of the resulting audio susceptibility is negative: an increase in input voltage will cause the output voltage to decrease. Figure 2-11e illustrates these behaviors when the input of the buck converter is stressed by a 6V variation. The upper curve depicts the output voltage for a critical ramp compensation. The voltage difference in the output envelope is only 10mV for a 6V input step, which leads to a (theoretical) ΔVout/ΔVin of −55dB. The middle curve shows how the response starts to degrade as additional ramp is added. The lower curve represents the error amplifier response when a slight ramp compensation is added. The decrease in the output voltage is clearly revealed by the rise in the error voltage.

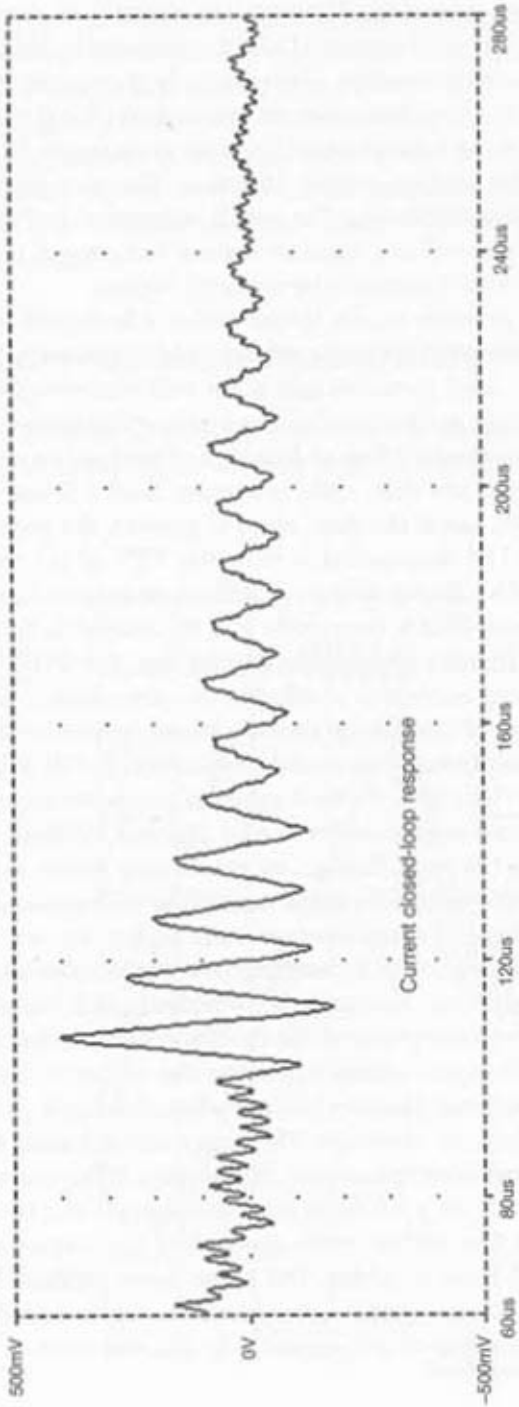


Figure 2-11c
A simple component arrangement shows the apparition of the Fsw/2 oscillations, which die out after a few cycles.

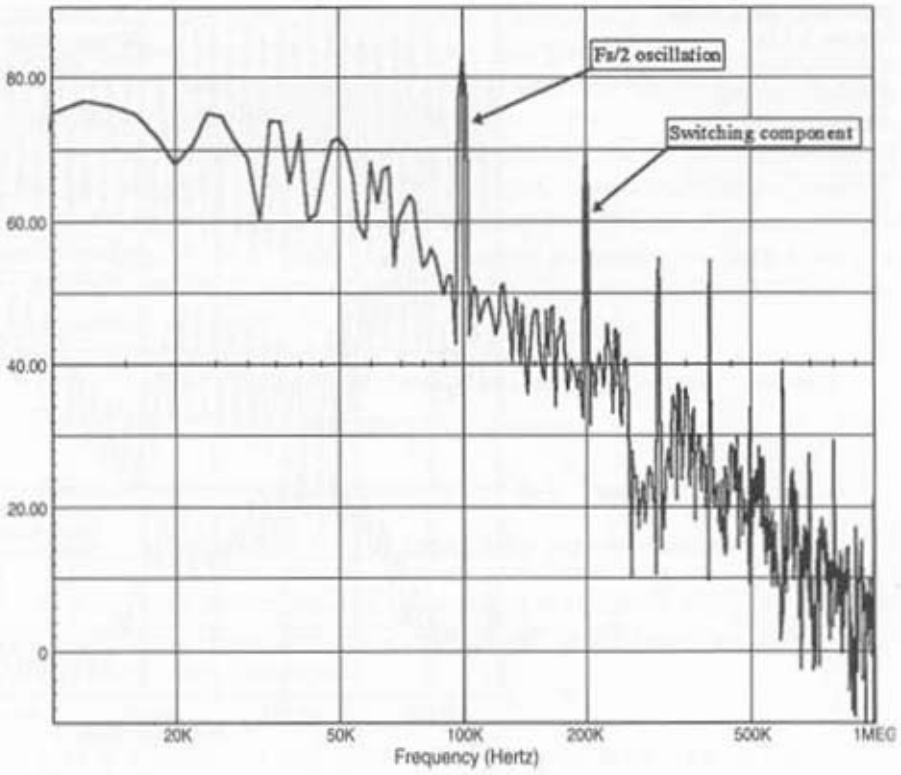


Figure 2-11d
In closed-loop configuration, poor ramp compensation can lead to permanent subharmonic oscillation at Fsw/2.

The Voltage Mode Model

The voltage-mode generic controller will follow the description given in Figure 2-12.

The architecture enables the inclusion of a current limitation circuit to reduce the on-time of the external power switch when its peak current exceeds a user-defined limit. This option is strongly recommended to make a rugged and reliable SMPS design that can safely handle input or output overloads. By simply connecting the ISENSE input to ground, you disable this option.

The Duty-Cycle Generation

In this model, the duty cycle is no longer controlled by the current information (except in limitation mode). It is controlled by the PWM modulator,

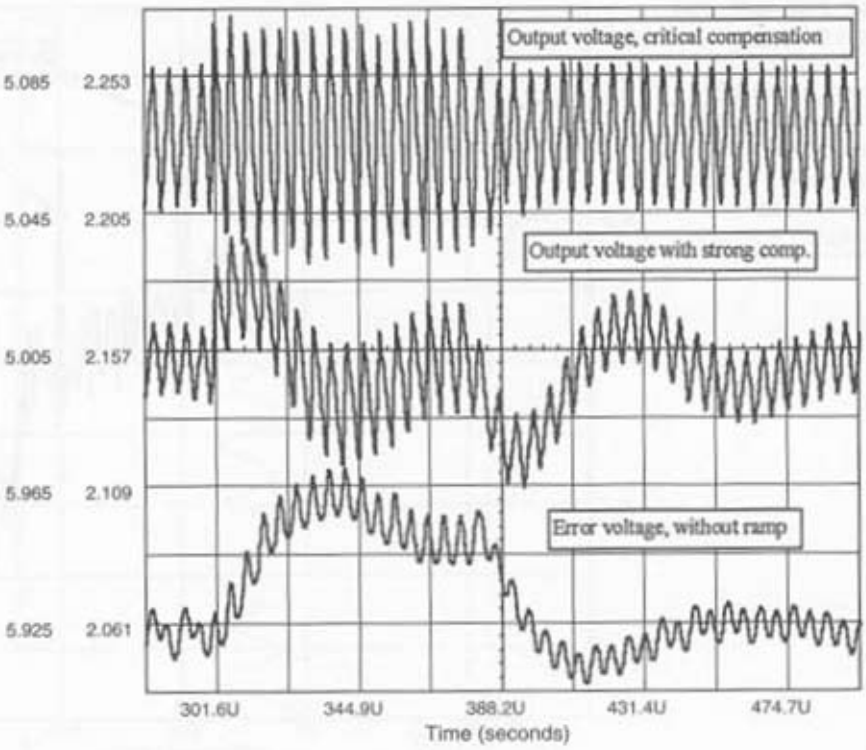


Figure 2-11e
The input ripple rejection is clearly affected by the compensation ramp.

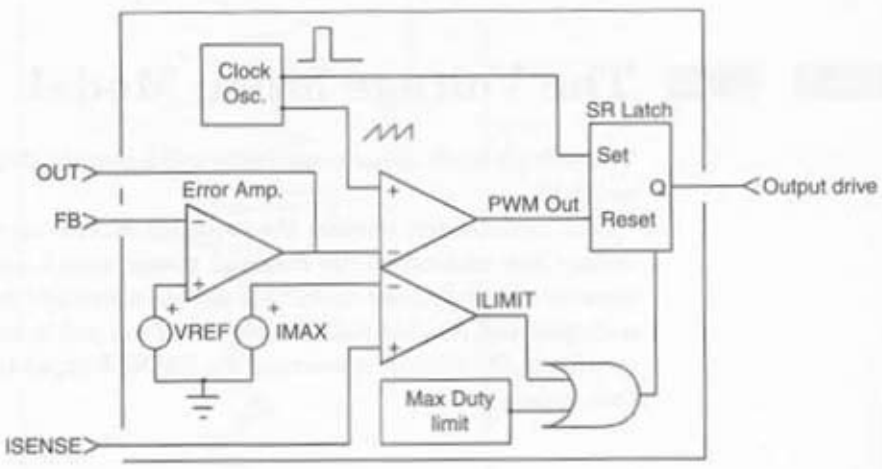


Figure 2-12
The voltage-mode model includes a current limitation for reliable designs.

which compares the error voltage with the reference sawtooth. The error amplifier output swing will then define the duty-cycle limits. Since this out-

put swing is user dependent, the model will calculate the peak-and-valley voltages of the reference sawtooth such that the chosen duty-cycle boundaries are not violated. Figure 2-13 depicts the well-known naturally sampled PWM modulator.

Since you will provide the main subcircuit with the duty-cycle limits and the error amplifier output swing, it is possible to calculate the corresponding sawtooth peak values, V_{valley} and V_{peak}. In CADENCE's PSpice or INTUSOFT's IsSpice, it is easy to define some particular variables with a .PARAM statement. The reading of the remaining lines in the netlist is then considerably simplified:

```
.PARAM VP = { (VLOW*DUTYMAX-VHIGH*DUTYMIN+VHIGH-VLOW)/(DUTYMAX-
+DUTYMIN) }
.PARAM VV = { (VLOW-DUTYMIN*VP)/(1-DUTYMIN)}
```

The sawtooth source then becomes:

```
VRAMP 1 0 PULSE {VV} {VP} 0 {PERIOD-2N} 1N 1N {PERIOD}
```

The OR gate that routes the reset signal to the latch from the PWM or the limitation comparator requires a simple in-line equation, followed by the classical delay network:

```
.SUBCKT OR2 1 2 3
E_B1 4 0 VALUE = { IF ( (V(1)>800M) | (V(2)>800M), 5V, 0 ) }
RD 4 3 100
CD 3 0 10P
.ENDS OR2
```

A Quick Example with a FORWARD Converter

Since the remaining elements have already been defined (comparators, error amplifier, and so forth), we are all set. The test circuit of Figure 2-14a is a forward converter that delivers 28V@4A from a 160V input source.

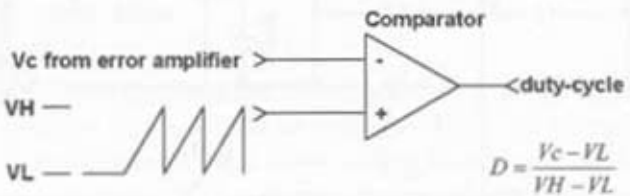


Figure 2-13
The model parameter will automatically adjust to satisfy the imposed duty-cycle limits.

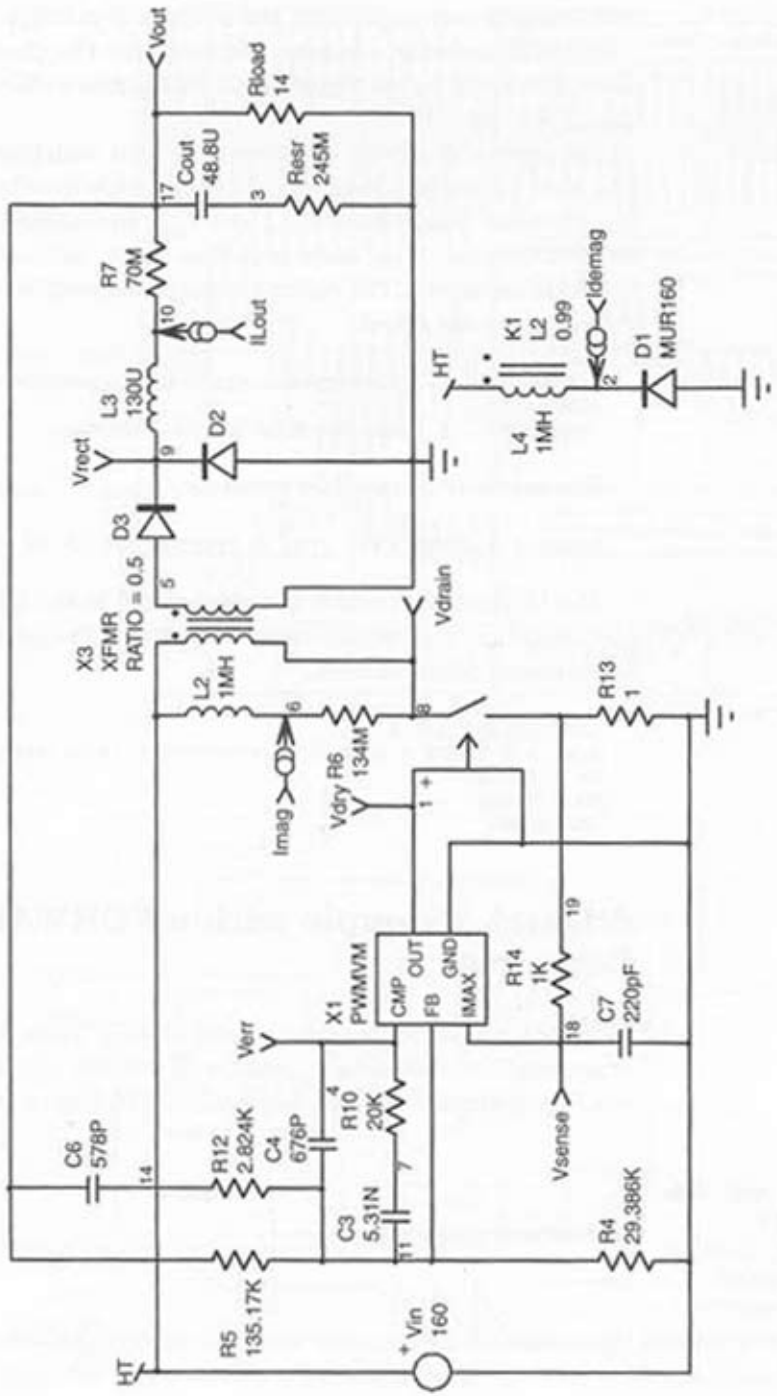


Figure 2-14a
A voltage-mode FORWARD converter built around the generic model

The switching frequency is set at 200kHz, with a maximum duty cycle of 0.45 because of the forward structure and the 1:1 power/demag turn ratio. Figure 2-14b depicts the curves that are obtained at start-up. The power switch is modeled with a smooth transition element, as provided by CADENCE and INTUSOFT. The error amplifier is pushed to its upper limit and needs some time to recover from this transient situation. This behavior is typical of the adopted compensation scheme for a voltage-mode converter that is operating in continuous mode.

Modeling with SPICE2

If you own a SPICE2 compatible simulator, you simply cannot use the B element syntax. To overcome this limitation, some equivalent (but more time-consuming) circuits can be constructed. The first generic function in our models is the perfect comparator. Figure 2-15a shows one solution. The unlabeled resistors provide a DC path to ground (10MEG).

The logical functions are less obvious, at least if you want to build something easily. The ideal gates in Figure 2-15b simulate quickly and converge well. They use the ideal SPICE2 voltage-controlled switch or the PSpice/IsSpice smooth transition switch.

The Flip-Flop is also translated to SPICE2 syntax, as the following lines explain.

```
**** FFLOP ****
.SUBCKT FFLOP 6 8 2 1
*       S R Q Q\
RDUM1 6 0 10MEG
RDUM2 8 0 10MEG
XINVS 6 6 10 NAND
XINVR 8 8 11 NAND
XNAQB 11 2 10 NAND
XNAQ 10 1 20 NAND
RD1 10 1 100

CD1 1 0 10P IC=5
RD2 20 2 100
CD2 2 0 10P IC=0
.ENDS FFLOP
****
```

```
**** 2 INPUT NAND ****
.SUBCKT NAND 1 2 3
 RDUM1 1 0 10MEG
RDUM1 2 0 10MEG
S1 3 5 1 0 SMD
S2 5 0 2 0 SMOD
RL 3 4 100
CD 3 0 10P
VCC 4 0 5V
.MODEL SMOD VSWITCH (RON=1
+ROFF=1MEG VON=3 VOFF=100M)
.ENDS NAND
```

Please note that the SPICE2 models are not declined for every structure, because this platform is outdated. They are offered to enable a "smooth" transition to SPICE2 users willing to migrate to SPICE3.

Again, we will not discuss the rest of the models in detail since they will be covered in dedicated sections.

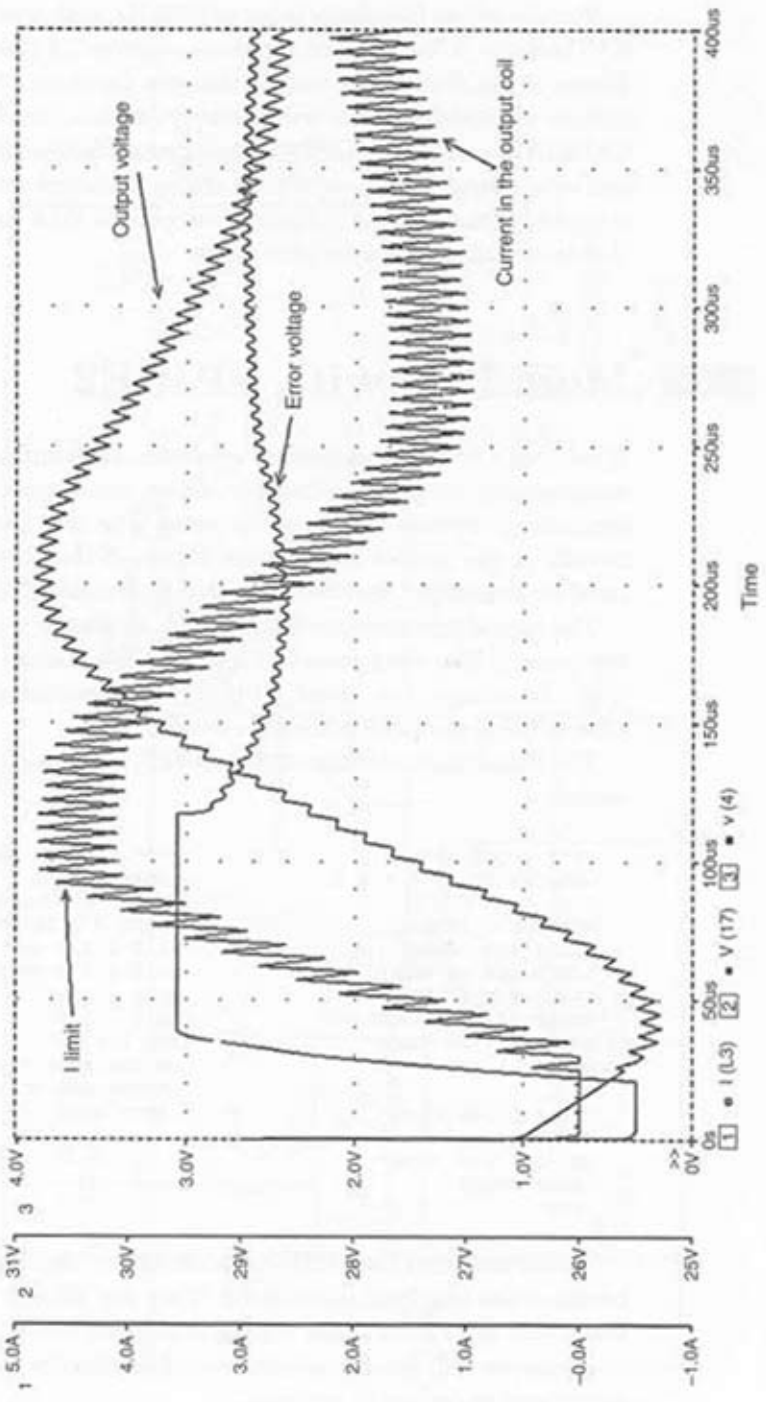


Figure 2-14b
Simulation results of the voltage-mode FORWARD converter.

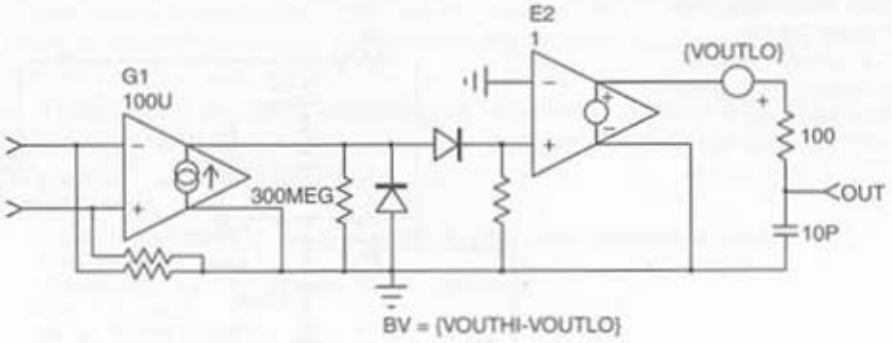


Figure 2-15a
A SPICE2 comparator enables the implementation of our generic models.

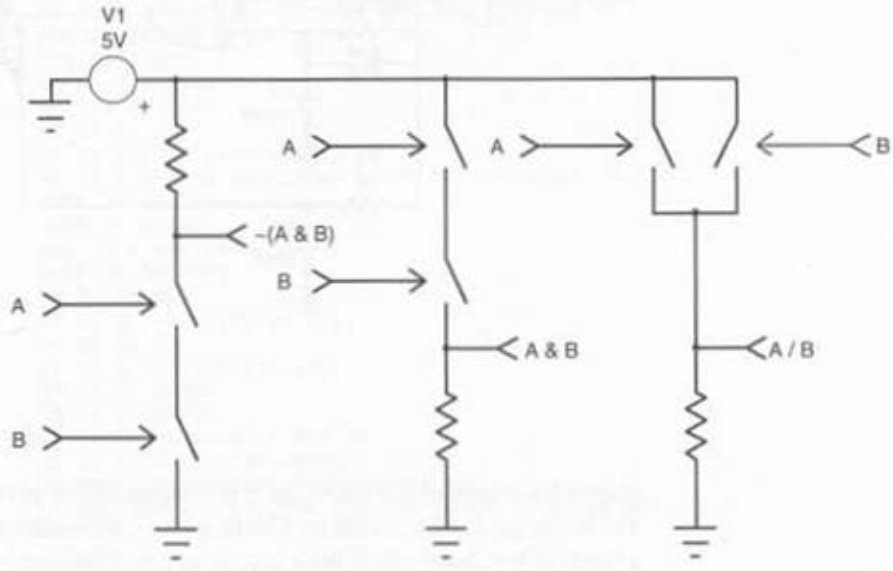


Figure 2-15b
By combining ideal switches, it is possible to combine simple logical functions.

Dead-Time Generation

Bridge or half-bridge designs using MOSFETs or IGBTs need some dead-time between the commutations to avoid any cross-conduction current spikes. This statement is also valid in SMPS implementing synchronous rectification. In a simulation environment, it is not always an easy task to write the stimuli so as to define a dead-time between commutations. Classical PULSE or PWL commands are unpractical, especially when either frequency or pulse width are changed during the simulation run. Figure 2-16a

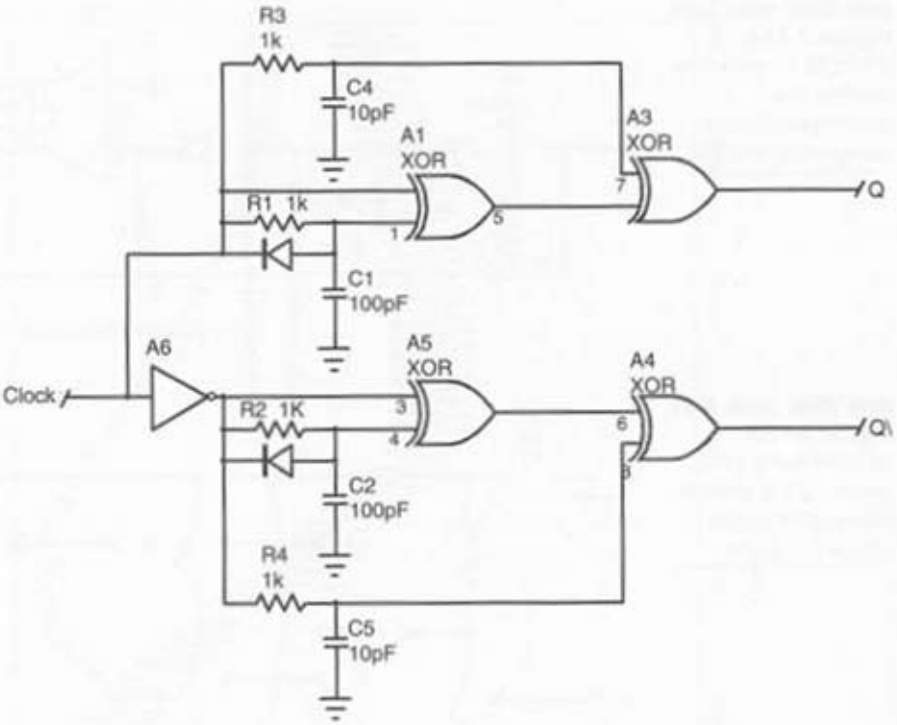


Figure 2-16a
The discrete solution to implement a dead-time generator.

shows the solution built around a few logical XOR gates. The principle uses the truth table of an XOR or XNOR gate, which states that its output is at a high or low level when both inputs are at different logical states:

An XOR Gate Truth Table

A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

This difference between the levels is made through the RC networks R1-C1 and R4-C5. The output of the A1-A5 gates thus delivers a short pulse

whose width is dependent upon the RC constant of its input network. This pulse will blank the signal delivered to the output, and thus it will generate the required dead-time.

These logical functions can easily be implemented using SPICE Analog Behavioral Modeling (ABM) features as demonstrated by the netlist given in the following (INTUSOFT example):

```
.SUBCKT DEADTIME 1 50 51 {DT=500N VHIGH=10V VLOW=100M RS=10}
* Clock_In Q Qbar
*Developed by Christophe BASSO (FRANCE)
RIN 1 0 1MEG
B6 17 0 V=V(1)>2V ? 10 : 0
R3 17 18 1k
C3 18 0 {DT/(1000*4.14)}
B4 21 0 V=V(25,19)<100MV ? {VLOW} : {VHIGH}
RCQ 21 60 100
CCQ 60 0 10P
BQ 61 0 V=V(60)
RSQ 61 50 {RS}
R4 22 23 1k
C4 23 0 {DT/(1000*4.14)}
B5 24 0 V=V(26,20)<100MV ? {VLOW} : {VHIGH}
RCQB 24 70 100
CCQB 70 0 10P
BQB 71 0 V=V(70)
RSQB 71 51 {RS}
R5 17 25 1k
C5 25 0 {DT/(1000*41.4)}
R6 22 26 1k
C6 26 0 {DT/(1000*41.4)}
D3 23 22 DISCH
D4 18 17 DISCH
B1 22 0 V=V(1)>2V ? 0 : 10
B2 19 0 V=V(17,18)<100MV ? 0 : 10
B3 200 0 V=V(22,23)<100MV ? 0 : 10
.MODEL DISCH D BV=100V CJO=4PF IS=7E-09 M=.45 N=2 RS=.8
+ TT=6E-09 VJ=.6V
.ENDS
```

The subcircuit needs to be fed with the dead-time value as well as the output high and low levels. The input clock is TTL-CMOS compatible. By changing B5 line to V=V(26,20)<100MV ? {VHIGH} : {VLOW}, the generator becomes suitable to drive a synchronous rectifier, as demonstrated by Figure 2-16b.

This is a very simplified example. We will discover later on how to combine this dead-time generator with one of the generic PWM controllers.

Figure 2-16c finally unveils the output signals delivered by the generator that clearly save the MOSFETs from any conducting overlap.

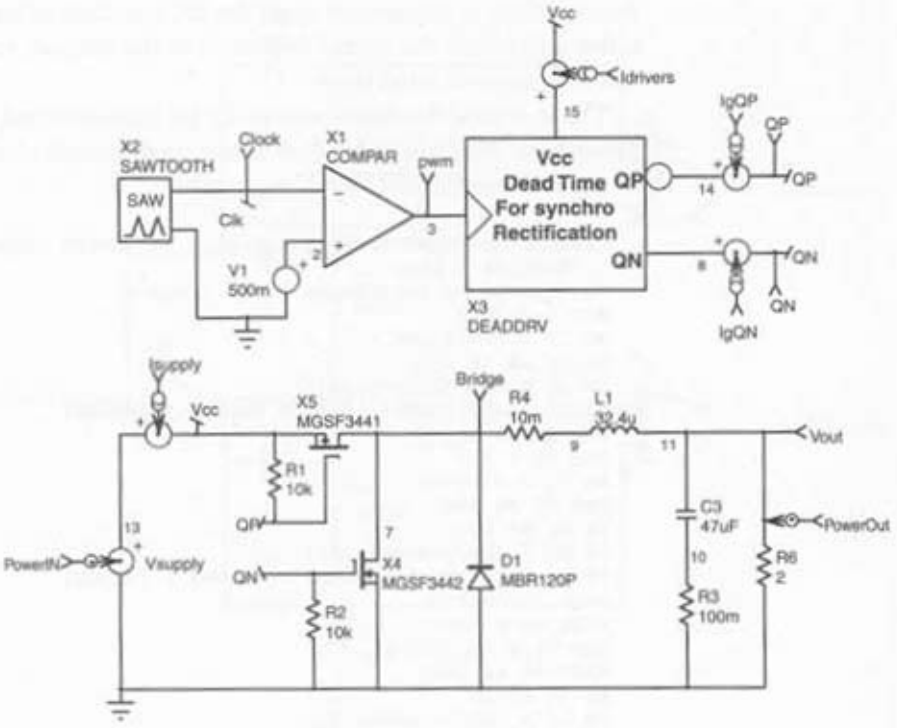


Figure 2-16b
A typical application schematic in synchronous rectification.

Dead-Time Generation with Delay Lines

To simplify the previous implementation, one can build a dead-time generator around delay line SPICE primitives. However, these commands are not always available, depending on the selected platform. Figure 2-17a depicts a possible solution. The input clock is routed via two delay lines featuring the same specs. When the clock goes high, one input of X2 AND is also high, but because of the delay line, the other input stays low for the given dead-time (DT). Once both inputs are high, the output delivers a logical 1 (Figure 2-17b).

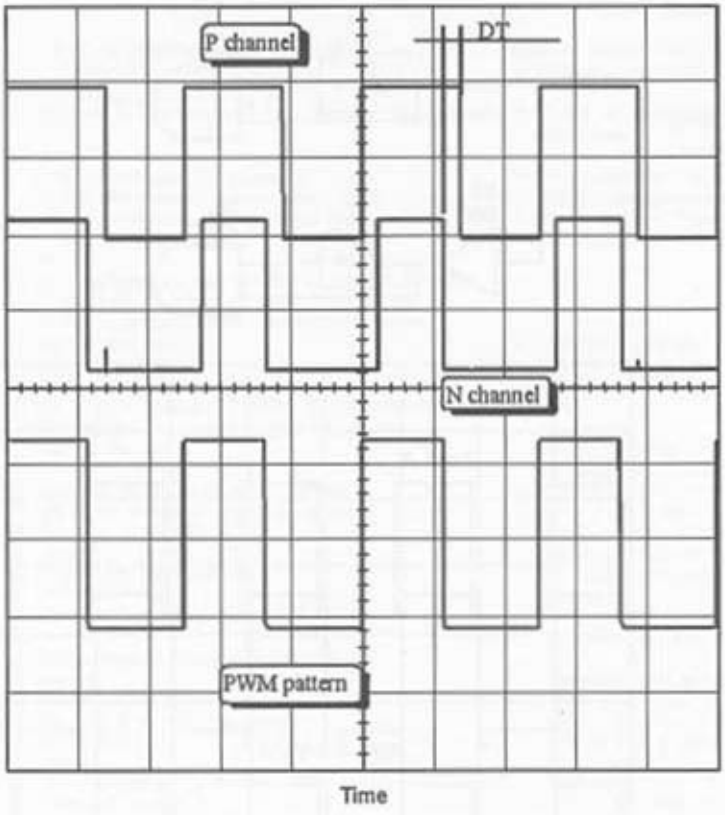
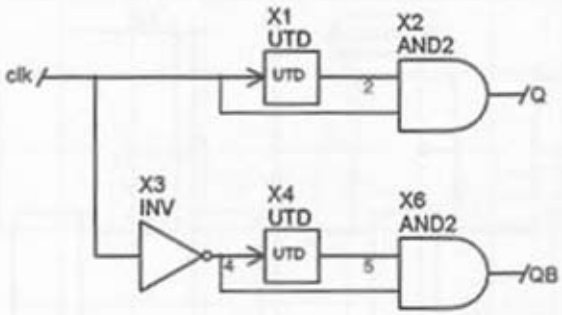


Figure 2-16c
This picture clearly shows the absence of overlap between cycles.

Thanks to common SPICE3 primitives like the delay lines (T), the translation of this generator can be implemented in a snapshot. The AND gate and the inverter are written with simple in-line equations.

Following are the netlists for a half-bridge driver with a floating upper output in both INTUSOFT's IsSpice4 and CADENCE's PSpice.



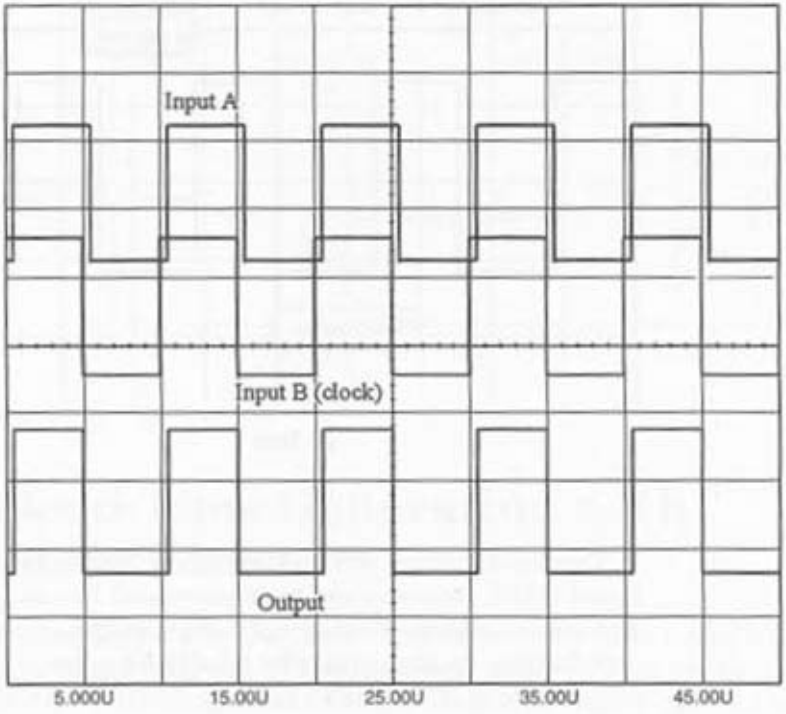


Figure 2-17a, Figure 2-17b
A simple way to generate a dead-time with two AND gates and delay lines.

IsSpice

```
.SUBCKT NEWDT CLK GU SU QL (DT=500N
+ VHIGH=10V VLOW=100M RS=10)
VLOW=100M RS=10
*Clock_In GateUpper SourceUpper GateLower
*
*DT: Deadtime in seconds
* VHIGH: Output level when high
* VLOW: Output level when low
* RS: Driver's output resistance
*
BU1 1 0 V=(V(CLK)>800M) & (V(TD1)>800M)
? {VHIGH} : {VLOW}  EBU1 1 0 VALUE =
{ IF ( (V(CLK)>800M) & (V(TD1)>800M),
BU2 4 SU V=V(1)
RSU 4 GU {RS}
RFLO SU 0 1G
BL 2 0 V=(V(CLKB)>800M) & (V(TD2)>800M)
? {VHIGH} : {VLOW}  RFLO SU 0 1G
RSL 2 QL {RS}

X1 CLK TD1 UTD PARAMS: TD=DT
X2 CLKB TD2 UTD PARAMS: TD=DT
X3 CLK CLKB INV
.ENDS
*INCLUDE DEAD.LIB
**********
.SUBCKT UTD 1 2 {TD=???}
*
*Parameters K=GAIN TD=DELAY
RIN 1 0 1E15
E1 3 0 1 0 1
T1 3 0 2 0 Z0=1 TD={TD}
R1 2 0 1
.ENDS
**** 1 INPUT INVERTER ****
.SUBCKT INV 1 2
B1 4 0 V=V(1)>800M ? 0 : 5V
RD 4 2 100


CD 2 0 10P
.ENDS INV
```

PSpice

```
.SUBCKT NEWDT CLK GU SU QL
+ PARAMS: DT=500N VHIGH=10

* Clock_In GateUpper SourceUpper
  GateLower
  *
* DT: Deadtime in seconds
* VHIGH: Output level when high
* VLOW: Output level when low
* RS: Driver's output resistance
*



+ {VHIGH}, {VLOW} ) }
  EBU2 4 SU VALUE = { V(1) }
  RSU 4 GU {RS}


  EBL 2 0 VALUE = { IF (
  (V(CLKB)>800M) & (V(TD2))800M),
+ {VHIGH}, {VLOW} ) }
   RSL 2 QL {RS}
   X1 CLK TD1 DL PARAMS: TD={DT}
   X2 CLKB TD2 DL PARAMS: TD={DT}
   X3 CLK CLKB INV
   .ENDS
   **********
   .SUBCKT DL 1 2 PARAMS: TD=500n
   *
   *Parameters K=GAIN TD=DELAY
    RIN 1 0 1E15
    E1 3 0 1 0 1
    T1 3 0 2 0 Z0=1 TD={TD}
    R1 2 0 1
    .ENDS
    **** 1 INPUT INVERTER ****
    .SUBCKT INV 1 2
    EB1 4 0 VALUE =
    { IF ( V(1)>800M,
    0 5V ) }
    RD 4 2 100
    CD 2 0 10P
    .ENDS INV
```

Typical applications include ½ bridge driver but also synchronous rectification. You can easily tailor any output polarity by reversing the corresponding SPICE element. For instance, if one wants to reverse the upper generator BU1, simply replace:

```
V=(V(CLK)>800M) & (V(TD1)>800M) ? {VHIGH} : {VLOW}
By
V=(V(CLK)>800M) & (V(TD1)>800M) ? {VLOW} : {VHIGH}
```

Figure 2-18a portrays a typical application in a simplified half-bridge driver while Figure 2-18b reveals the corresponding waveforms.

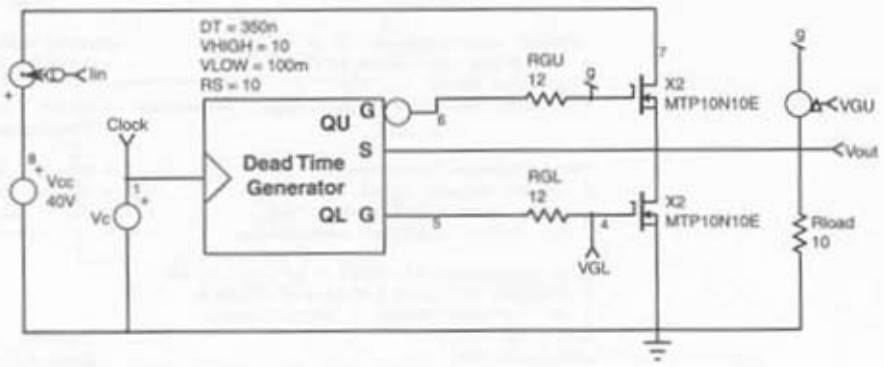


Figure 2-18a
A typical half-bridge application implementing two N-channels.

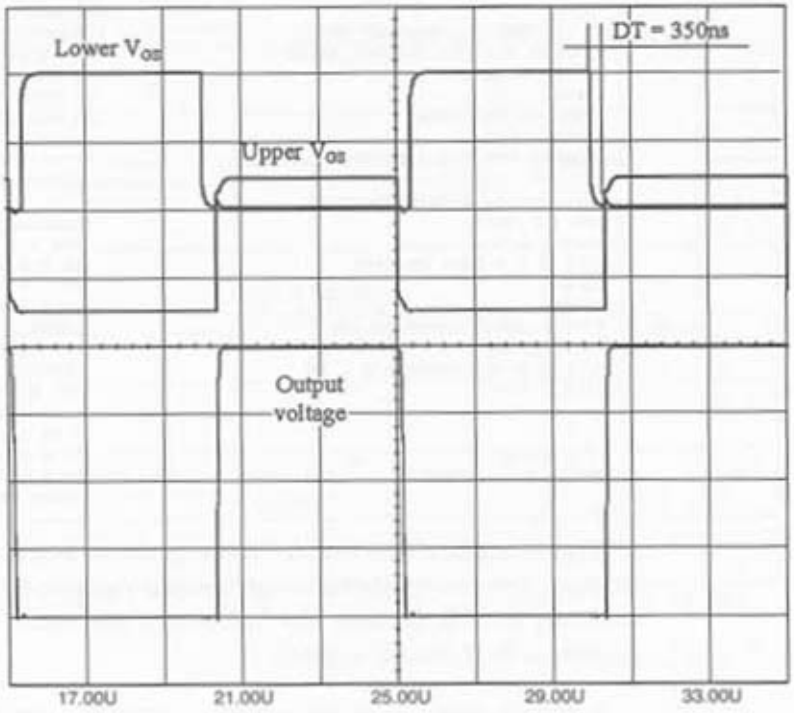


Figure 2-18b
Resulting IsSpice4 waveforms.

By using delay lines SPICE primitives rather than RC networks, the resulting dead-time generation gains in precision.

Convergence Options

As any mathematical tool looking for a solution, SPICE can sometimes fail to converge. Without detailing why this can happen (reference [30] does it thoroughly), we give in the following section some options that you can use to tweak SPICE parameters and make the simulator finally converge:

TRANSIENT Simulations

.options RELTOL = 0.01 (default = 0.001)	RELTOL sets the relative error tolerance for convergence. It also obviously affects the simulation speed. You can relax it down to 1% (0.01) for power simulation where less precise results are needed.
.options ABSTOL = 1µA (default = 1pA) .options VNTOL = 1mV (default 1µV)	ABSTOL and VNTOL respectively define the absolute voltage and current error tolerances. Once RELTOL has been defined, you need to evaluate the smallest current and voltages present in your circuit. Then apply the following relationship to set ABSTOL and VNTOL: ABSTOL = RELTOL * Smallest_current VNTOL = RELTOL * Smallest_voltage
.options GMIN = 100p (default = 1p)	GMIN ensures that a differential voltage applied across an active component always forces a minimum of differential current to flow through it. If a device would present an infinite conductance (di/dv = 0), the iteration algorithm would simply fail. Typical relaxing values are 1n or 10n.
.options ITL1 = 1k (default = 100)	ILT1 is used to increase the DC iteration limit. This is the number of iterations SPICE will perform before giving up during the bias point calculation. If you have a message like "NoConvergence in DC analysis," then you should consider raising ITL1 to 1k.

.options RSHUNT = 10Meg (default = 0)	Implemented by IsSpice4, this options asks SPICE to wire a resistor of RSHUNT ohms from every node to ground, thus always offering a DC path to ground.

AC Simulations

AC simulations are less prone to nonconvergence problems. However, the simulator can fail during the bias point calculation. If you use B elements or other behavioral sources, be sure that no division by zero can take place. You can easily avoid that by adding some offset to any denominator: V = V(3)/V(8) → V = V(3)/(V(8)+1µ.). .options ITL1 = 1k can also help in finding the good DC bias point.

CHAPTER 3

Topology-by-Topology Simulation Recipes

Introduction

The goal of this book is to provide you with ready-to-simulate templates where you will copy-paste your component values. We have tried to cover a large variety of topologies, mainly those derived from the BUCK, BOOST, and BUCK-BOOST structures. Because it is impossible to offer an exhaustive list of examples, we believe that the information contained in this book will enable you to build your specific architecture. We have strived to derive the models and application schematic into IsSpice, PSpice, and Spectrum-Software's MicroCap. Some examples will run with the demo version; some will require the full version to execute. The exact CD-ROM content is detailed later on.

With this chapter, we finally get to the heart of the matter: simulating a given topology. Each subsection contains

- *How it works:* A brief description of the circuit concept
- *Equations:* An array that summarizes the main design equations
- *Averaged:* An average simulation in both AC and TRANsient
- *Switched:* A complete switched-application example.

Thanks to the following examples, you will learn how to conduct measurements in order to evaluate the following key parameters:

AC Input impedance: Open/Closed loop

AC Output impedance: Open/Closed loop

AC, TRAN Audio susceptibility: Open/Closed loop

AC Vout/Control open-loop function

However, they will be scattered among the numerous examples, rather than repeating every measurement step for each topology.

As we said in Chapter 1, "Overview," we have selected two models for our average simulations: Ridley and Ben-Yaakov GSIM models. Because Ridley's only work is in AC and cannot find their DC point alone, we will employ them in duality with GSIM in current-mode systems only. For the voltage-mode simulations, GSIM models will be solely used.

Because simulations *always need* to be confronted with external analytical calculations, an array summarizes the basic equations for the given topology and particularly the pole and zero locations. Sometimes the equation expressions are too complicated to fit this array and are replaced by a reference number where the information is fully detailed. Nevertheless,

before going further, we need to detail and understand some universal key parameters of our converters.

Please note that the design examples have all been calculated using the powerful POWER 4-5-6 Design Engine developed by RIDLEY Engineering [13].

The Critical Inductance

As was previously depicted by Figure 1-7d and 1-7e, the inductor can be the seat of different situations: continuous current or discontinuous current. As you will see, two black boxes are operating at exactly the same condition, one in DCM while the other one forces CCM, exhibit drastic dynamic differences. Thus, it is very important to define the boundary at which your supply crosses the mode.

Where Is the Boundary?

There are three ways you can think of the boundary between the modes. One is the critical value of the inductance, L_C, for which the supply will work in either CCM or DCM given a fixed nominal load. The second deals with a known inductance L: what level of load, R_C, will push my supply into CCM? Or what minimum load should my SMPS see before entering DCM? The third one uses fixed values of the previous elements but adjusts the operating frequency, F_C, to stay in critical conduction. These questions can be answered after a few lines of algebra corresponding to Figure 3-1a's example, a FLYBACK converter.

To help determine some key characteristics of this converter, we will refer to the following statements:

- The average inductor voltage per cycle should be null (a).
- From Figure 1-7e, when $L = L_C$, $I_{L(avg)} = \frac{1}{2} \cdot Ip$ (b).
- A 100% efficiency leads to Pin = Pout (c).

The DC voltage transfer ratio in CCM is first determined using statement (a), thus equating Figure 3-1b's areas: $Vdd \times N \times D = Vo \times (1 - D)$. After factorization, it comes out as $\frac{Vout}{Vin} = \frac{D}{(1 - D)} \times N$ (eq. 2.1).

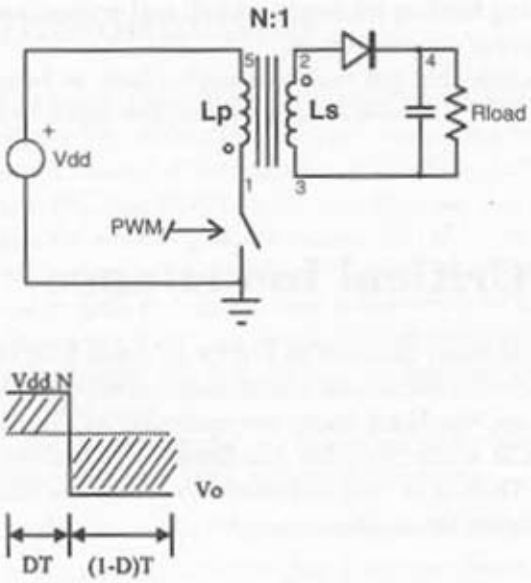


Figure 3-1a, Figure 3-1b A FLYBACK converter and its associated operating (secondary) waveforms.

As we can see from Figure 1-7e, the flux stored in the coil during the ON time is down to zero right at the beginning of the next cycle when the inductance equals its critical value (L = L_C). Mathematically, this can be expressed by rewriting the formula $V_L = L \cdot \frac{dI_L}{dt}$, and equating both half sides of the triangle:

- $V_L \times dt = L \times dI_L$ thus, $\int_0^{\beta} V_L \cdot dt = Lc \cdot \int_0^{I_P} dI_L$. (eq. 2.2)
- $\frac{Vin \times D}{Fs} = Lc \times Ip = 2 \times I_{L(avg)} \times L_C$, from (b).(eq. 2.3)
- From (c), $Vin \times I_{L(avg)} = Io \times (Vin \times N + Vout)$, or $I_{L(avg)} = Io \times \left(N + \frac{Vout}{Vin}\right)$.(eq. 2.4)
- By definition, $I_O = \frac{Vout}{R}$ and $Vout = Vin \times N \times \frac{D}{1-D}$ from (eq. 2.1).

If we introduce these elements in the above equations, we can solve for the critical values of R_C and L_C:

$$R_C = \frac{2 \times L_C \times Fs \times N^2}{(1-D)^2} \text{ (eq. 2.5)} \qquad L_C = \frac{R_C \times (1-D)^2}{2 \times Fs \times N^2} \text{ (eq. 2.6)}$$

This is for the FLYBACK converter, but we can easily gather the critical values for the remaining topologies [15]. (See Table 3-1.)

When the Deadtime Vanishes . . .

The FLYBACK converter, as with the BOOST and BUCK-BOOST structures, features an operating mode comparable to someone filling a bucket (coil) with water and flushing it into a water tank (capacitor). The bucket is first presented to the spring (ON time) until its inner level reaches a defined limit. Then the bucket is removed from the spring (OFF time) and flushed into a water tank that supplies a fire engine (load). The bucket can be totally emptied before refilling (DCM), or some water can remain before the user presents it back to the spring (CCM). Let's suppose that the man is experienced and is certain that the recurrence period (ON+OFF time) is constant. The end-user is a fireman who closes the feedback loop via his voice, shouting for more or less flow for the tank. Now, if the flames suddenly get bigger, the fireman will require more power from its engine and will ask the bucket man to provide the tank with a higher flow. In other words, the bucket operator will fill his container longer (ON time increases). However, because by experience he keeps his working period constant, the time he will spend flushing into the tank will naturally diminish (OFF time decreases), as will

Table 3-1

Critical Inductance and Load Values for Various Topologies.

Topology	L_C	R_C
BUCK FORWARD	$\frac{(1-D)\cdot Rload}{2\cdot Fsw}$	$\frac{2\cdot Fsw\cdot L}{(1-D)}$
BOOST	$\frac{Rload\cdot D\cdot(1-D)^2}{2\cdot Fsw}$	$\frac{2\cdot L\cdot Fsw}{D\cdot(1-D)^2}$
BUCK-BOOST	$\frac{Rload\cdot(1-D)^2}{2\cdot Fsw}$	$\frac{2\cdot L\cdot Fsw}{(1-D)^2}$
FLYBACK (primary inductance)	$\frac{Rload\cdot(1-D)^2}{2\cdot Fsw\cdot N^2}$	$\frac{2\cdot L\cdot Fsw\cdot N^2}{(1-D)^2}$

Rload: load resistance
Fsw: switching frequency
D: duty-cycle
L: inductor

the amount of water poured. The fire engine will run out of power, making the fireman shout louder for more water, extending the filling time, and so on. The loop oscillates!

This behavior is typical for converters in which the energy transfer is not direct (unlike the BUCK-derived families); this severely affects the overall dynamic performances. In time domain, a large step-load increase requires a corresponding percentage rise of the inductor current. This necessitates a temporary duty-cycle augmentation that (with only two operational states) causes the diode conduction time to diminish. Therefore, it implies a decrease in the average diode current at first, rather than an increase as desired. When heavily into the continuous mode and if the inductor current rate is small compared to the current level, it can take many cycles for the inductor current to reach the new value. During this time, the output current is actually reduced because the diode conduction time (T_{OFF}) has been decreased, even if the peak diode current is rising. In DCM, by definition, a third state is present when neither the diode or the switch conduct and the inductor current is null. This "idle time" (also called dead-time) enables the switch duty cycle to lengthen in the presence of a step-load increase without lowering the diode conduction time. In fact, it is possible for the DCM circuit to adapt perfectly to a step-load change of any magnitude in the very first switching period with the switch conduction time, the peak current, and the diode conduction time all increasing at once to the values that will be maintained forevermore at the new load current.

The extra delay is mathematically described by a *Right Half-Plane Zero* (RHPZ) in the transfer function $\left(Av = \frac{(1 - s_{z1}) \times \ldots}{\ldots}\right)$ which forces the designer to roll off the loop gain at a point where the phase margin is still secure. A classical zero in the Left Half-Plane $\left(Av = \frac{(1 + s_{z1}) \times \ldots}{\ldots}\right)$ provides a *boost* in gain AND phase at the point it is inserted. Unfortunately, the RHPZ gives a boost in gain, but lags the phase. More viciously, its position moves as a function of the load, which makes its compensation almost an impossible exercise. Rolling off the gain well under the worse RHPZ position is the usual solution. Let's also point out that the low-frequency RHPZ is only present in FLYBACK type converters (BOOST, BUCK-BOOST) operating in CCM and moving to higher frequencies (then becoming negligible) when the power supply enters DCM. The loop compensation becomes easier. For additional information, reference [16] gives an interesting *experimental* solution to cure the BOOST from its low-frequency RHPZ, while

reference [17] presents an integrated solution to force DCM in any conditions. The RHPZ position will be given by topology later on.

After this introduction to the delicacies of the CCM, let's have a look at the BOOST Voltage Mode.

BOOST Voltage Mode

The BOOST converter is presented in Figure 3-2a. For rugged voltage-mode designs, we strongly encourage you to monitor the peak inductor current and make sure it always stays within the safe limits of the switch.

How It Works

When the switch closes, Vin is applied to the inductor L, and D's anode is stuck to ground. As a matter of fact, the current ramps up with a slope of $\frac{Vin}{L}$ (eq. 2.7) toward its final peak value Ip. When the switch opens (for example, because of the PWM order), the magnetic field inside the inductor collapses, and in attempt to keep the amps-turns constant, its voltage reverses. The current is now delivered to the load and capacitor, ramping down from Ip with a slope of $\frac{Vout - Vin}{L}$ (eq. 2.8). An easy way to find the transfer function of any converter is to apply the fact that the inductor average voltage across one switching cycle is null. If we stick to this rule and transfer it to Figure 3-2a, it becomes: $\overline{Vin} - \overline{Vout} = 0$ (eq. 2.9). $Vout_{avg}$ is

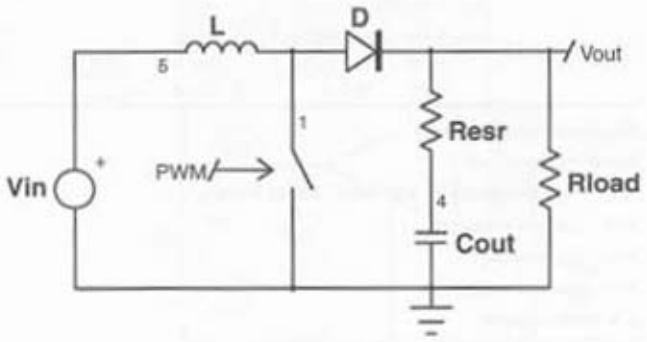


Figure 3-2a
A classical BOOST converter

simply $Vout_{peak} \times \frac{toff}{Tsw}$ or $Vout_{peak} \times (1 - D)$ (eq. 2.10). By equating Vin and eq. 2.10, we obtain the open-loop transfer function: $\frac{Vout}{Vin} = \frac{1}{1 - D}$ (eq. 2.11).

Equations

Following are the equations for a voltage-mode control BOOST converter operating in CCM or DCM. These equations, as well as the ones later given, are a compilation of results found in references [15, 19, 20, 21] (See Table 3-2.)

Table 3-2

BOOST Voltage-Mode Equations.

	DCM	CCM
1st-order pole	$\frac{2 + \frac{1}{\sqrt{1 + \frac{4 \cdot D^2}{J}}}}{2 \cdot \pi \cdot Rload \cdot Cout}$	
2nd-order pole	High frequency pole, see reference [5]	$\frac{(1 - D)}{2 \cdot \pi \cdot \sqrt{L \cdot C_{out}}}$
Left Half-Plane Zero	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [5]	$\frac{(1 - D)^2 \cdot R}{L}$
V_{output}/V_{input} DC Gain	$\frac{1 + \sqrt{1 + \frac{2 \cdot D^2 \cdot Rload}{L \cdot Fsw}}}{2}$	$\frac{1}{(1 - D)}$
V_{output}/V_{error} DC Gain	$\frac{Vin}{\sqrt{J}} \cdot \frac{\sqrt{1 - \frac{Vin}{Vout}}}{1 - \frac{Vin}{2 \cdot Vout}}$	$\frac{Vout^2}{Vin}$

F_{sw} = switching frequency
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
Cout = output capacitor
Vin = input voltage
Vout = output voltage
L = main inductor
D = duty-cycle
J = 2 · L · Fsw / R

Averaged

Our design implements a 12W BOOST converter operating in DCM at 200kHz. Figure 3-2b details the components arrangement for an AC simulation. The model uses the GSIM BOOSTVM available in both IsSpice and PSpice. The loop is opened by wiring the LOL and COL components as previously described. As you can see on Figure 3-2b, we have called the DC points from IsSpice and printed them on the schematic. They reveal a 12V value—it is what we had exactly been hoping for: a duty-cycle of 27%. The error amplifier is a macro-model as depicted in the generic model section. Please note the presence of D2, which is not mandatory, but instead forces the loop to account for its forward loss. D2's incremental resistance (which depends on the output current) will also play a significant role in the out-

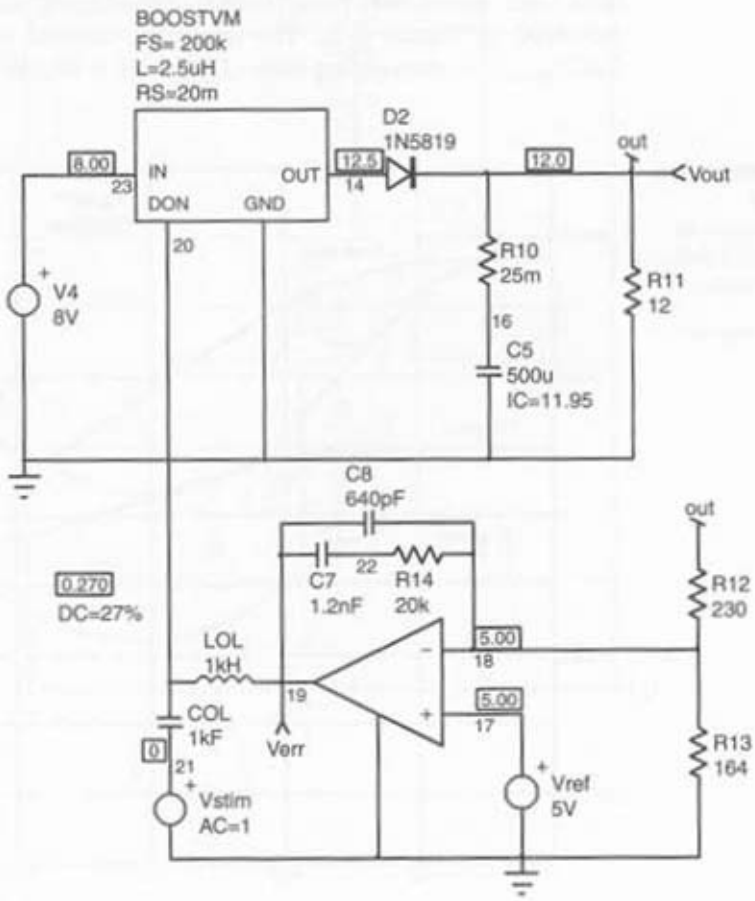


Figure 3-2b
The average voltage-mode BOOST simulation template.

put impedance. The simulation results are shown in Figure 3-2c and reveal a (theoretical) bandwidth of 52kHz thanks to the compensation network calculated by POWER 4-5-6. The phase margin is also comfortable with a 45° value at 0dB.

Switched

The switched version gathers our generic model and some semiconductors as the main switch associated with the rectifier diode. Figure 3-2d depicts the simulation file.

Different kinds of simulations can be run, but our interest lies in the steady-state phase where the system actually regulates the output. For that purpose, an *.IC* SPICE statement forces Cout's voltage to be close to the final value upon start-up. This trick ensures a minimum of switching pulses (and thus simulation time) before entering regulation. The results are delivered in Figure 3-2e. The capacitor current ripple is evaluated at $1.36A_{RMS}$, thus dissipating $Resr \cdot I_{RMS}^2 Cout = 46mW$.

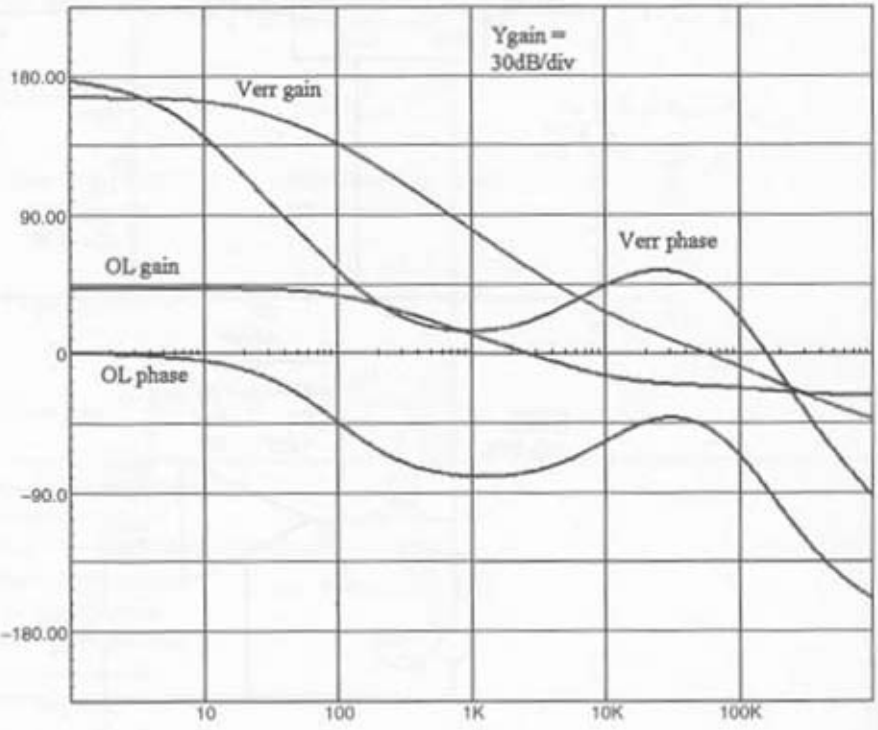


Figure 3-2c
Simulation results in *open-loop* (OL) after the compensation network.

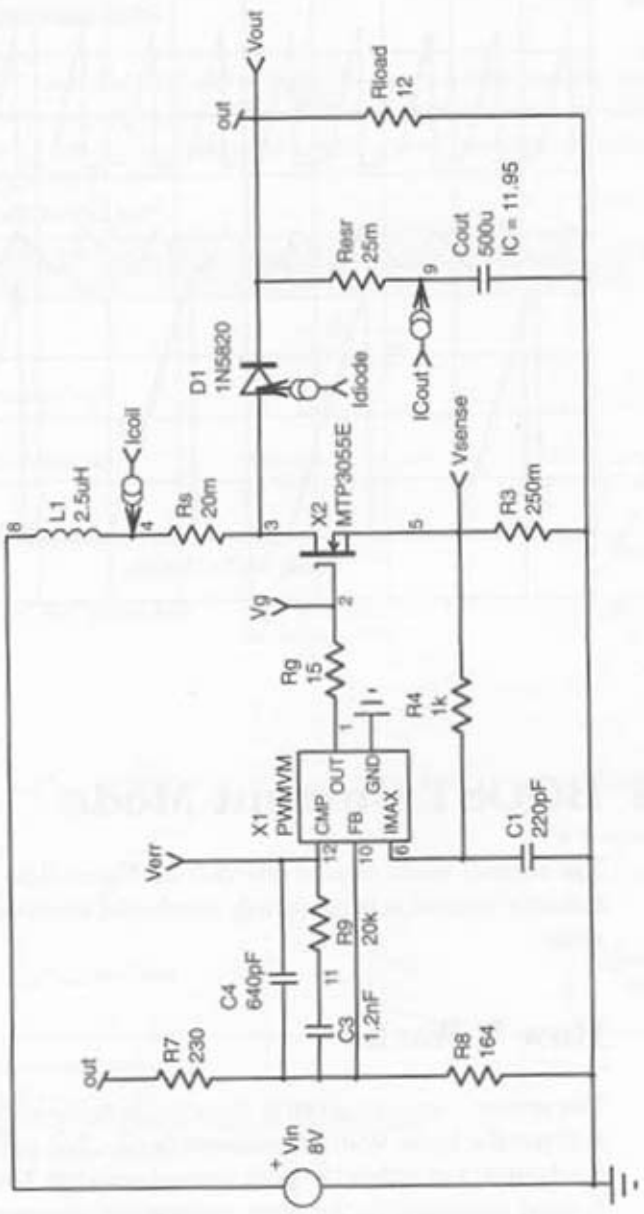


Figure 3-2d
Our switched BOOST simulation template.

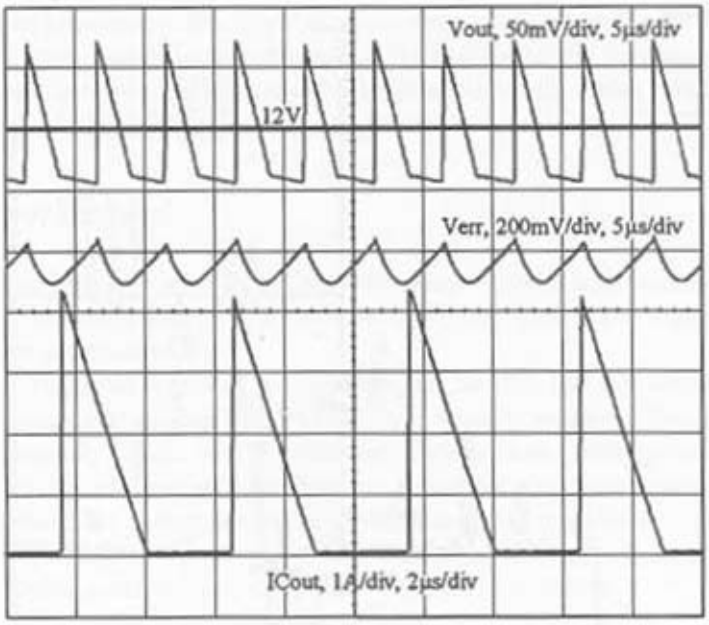


Figure 3-2e
The final steady-state simulation results.

BOOST Current Mode

The current mode version differs from Figure 3-2a in such a way that the inductor current is permanently monitored to actually determine the duty-cycle.

How It Works

The general remarks given in the voltage mode section still hold. However, it is not the Pulse Width Modulator device that naturally stops the switch conduction, but rather the peak current setpoint. This peak current setpoint is fixed according to the error voltage and varies with the output power demand. A resistive element usually measures the current that flows in the main switch. This element (called Ri in the AC model) fixes the current loop gain. However, some ramp compensation might be needed to compensate for eventual subharmonic oscillations.

Equations

Below are the first-order equations for a current-mode control BOOST converter operating in CCM or DCM. These equations, as well as the ones later given, are a compilation of results found in references [15, 19, 20, 21]. (See Table 3-3.)

Table 3-3

Boost Current-Mode Equations.

	DCM	CCM
1st-order pole	$\frac{2+\frac{1}{\sqrt{1+\frac{4\cdot D^2}{J}}}}{2\cdot\pi\cdot Rload\cdot Cout}$	$\frac{1}{\pi\cdot Rload\cdot Cout}$
2nd-order pole	High frequency pole, see reference [5]	None because of current mode
Left Half-Plane Zero	$\frac{1}{2\cdot\pi\cdot R_{ESR}\cdot C_{out}}$	$\frac{1}{2\cdot\pi\cdot R_{ESR}\cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [5]	$\frac{(1-D)^2\cdot Rload}{L}$
V_{output}/V_{input} DC Gain	$\frac{2+\frac{1}{\sqrt{\frac{1}{4}+\left[\frac{k\cdot Vc}{Vin}\right]^2\cdot\frac{1}{J}}}}{Rload\cdot Cout}$	$\frac{1}{(1-D)}$ if we introduce k: $Vout=\sqrt{k\cdot Vc\cdot Rload\cdot Vin}$
V_{output}/V_{error} DC Gain	$\frac{k}{\sqrt{J}}\cdot\frac{\sqrt{1-\frac{Vin}{Vout}}}{1-\frac{Vin}{2\cdot Vout}}$	$\frac{k}{2}\cdot\frac{Rload\cdot Vin}{Vout}$

F_{SW} = switching frequency
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
Cout = output capacitor
Vin = input voltage
Vout = output voltage
L = main inductor
Vc = control voltage
k = max. Ipeak / max. Vc
Ipeak = k · Vc
J = 2 · L · Fsw / Rload

Averaged

The design example depicts a BOOST converter delivering 6V@6W to an RF Power amplifier from a single Lithium-Ion battery (Vin = 2.7V to 4.8V). The parameters calculated by POWER 4-5-6 are the following:

Fsw = 200kHz

L = 2.5µH

Cout = 500µF, 25mΩ ESR

Rsense = Ri = 300mΩ

Rload = 6Ω

Figure 3-3a portrays the typical way to wire the Ridley BOOST CCM model. However, it is important to be sure that the converter operates in CCM. By applying the critical inductance formula $Lc = \frac{R \cdot D \cdot (1 - D)^2}{2 \cdot Fsw}$, we can determine if we are really CCM: Lc = 1.74µH (value under which we are DCM) < 2.5µH → CCM okay.

Despite the apparent complexity of its description, the implementation does not represent a major problem. The parameters are obvious because you feed the model with what you calculated. The only drawback lies in the fact that the model cannot find its DC point alone. You therefore need to pass the output (load, Vout, etc.) and also the input conditions. Once set, add a stimulus source on the Ctrl pin and watch for the output. The result is delivered in Figure 3-3b. In lack of compensation ramp (mc = 1), the Fsw/2 peaking is well pronounced.

OUTPUT IMPEDANCE If the output impedance is interesting for your application, simply put Vstim to 0 and wire a current source on the output as Figure 3-3c indicates. By setting this source to 1A, plotting Vout/Iout immediately gives you ohms. If you take 20 . log of the result, you compress everything into dBΩ: 0dBΩ = 1Ω, 60dBΩ = 1kΩ.

Adding the feedback loop with the adequate shaping elements lets you easily compare the open-loop versus closed-loop results.

The closed loop output impedance is defined by $Zout_{CL} = \frac{Zout_{OL}}{1 + T_{OL}}$. Since the open-loop gain T_{OL} diminishes with frequency, the output impedance rises as long as the frequency increases. This behavior describes an inductive output impedance which, in certain cases, can lead to annoying resonances (Figure 3-3d).

Figure 3-3a
The RIDLEY model does not present any difficulty of use.

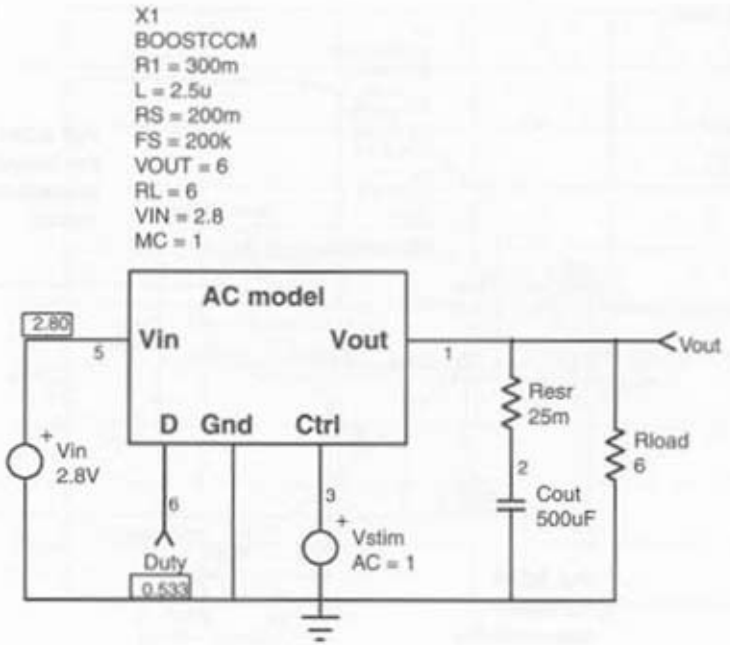
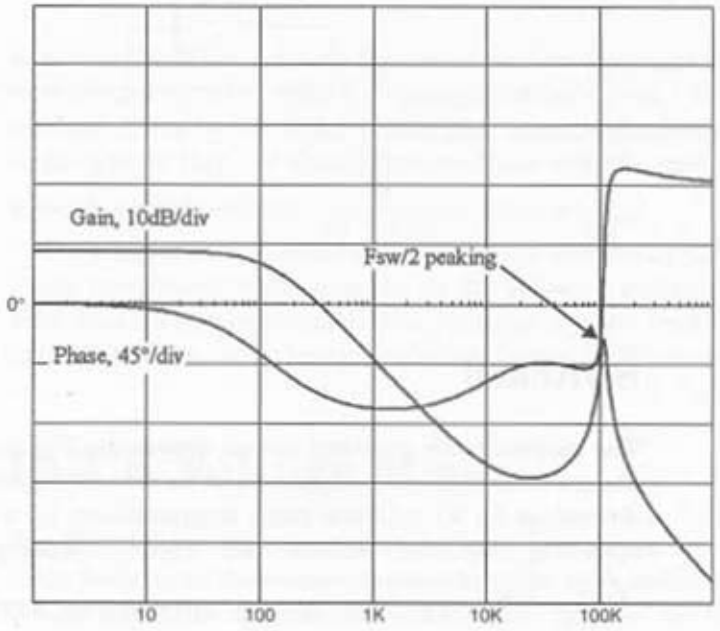


Figure 3-3b
No ramp compensation reveals subharmonic instability.



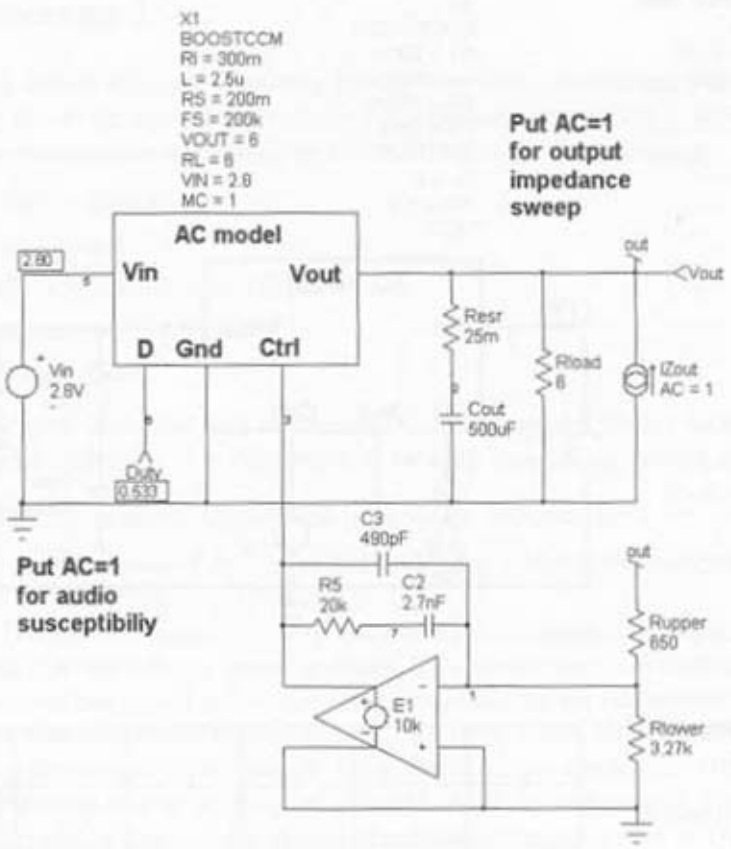


Figure 3-3c
This sketch shows how to carry a closed-loop output impedance study.

Switched

The current-mode switched circuit appears in Figure 3-3e, directly using the previous example components. If we want to inject 50% of the inductor downslope for an optimum ramp compensation, let us calculate the corresponding summing resistor we need: Downslope is during T_{OFF}: $\frac{Vout - Vin}{L} = 1.28A/\mu s$. 50% is 640mA/µs or 3.2A over 5µs (200kHz

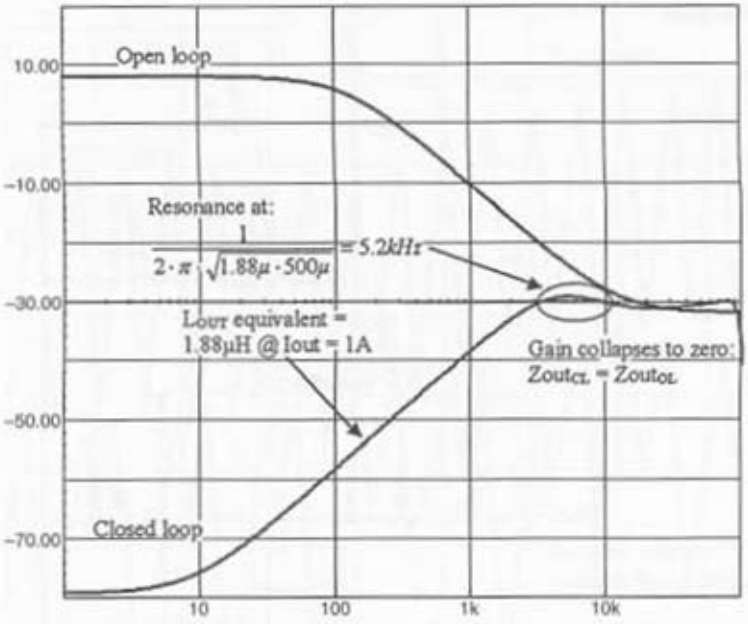


Figure 3-3d
Results show how Zout increases with the frequency: it behaves like a coil, which can finally combine with Cout (here at 5.2kHz)!

switching frequency). Using Rsense to convert into volts leads to a final level of 3.2A · 0.3Ω = 960mV. To generate 960mV from a 5V ramp voltage, we must divide by 5.2. If the resistor that conveys the sense information is selected to be 1kΩ, the Vramp this combines with the current information through a 4.2kΩ resistor: $\frac{1k}{1k + 4.2k} = 192m = \frac{1}{5.2}$.

The effect of ramp compensation is clearly revealed by the absence of the Fsw/2 component when zooming on the inductor current signal (Figure 3-3f). This result was obtained after pulsing the input level from 3.3V down to 2.8V, once the converter has stabilized (using a PWL statement).

BUCK Voltage Mode

The BUCK converter is presented in Figure 3-4a. Again, for rugged voltage-mode designs, we recommend a pulse-by-pulse peak inductor current monitoring to make sure it never exceeds the safe limits of the switch.

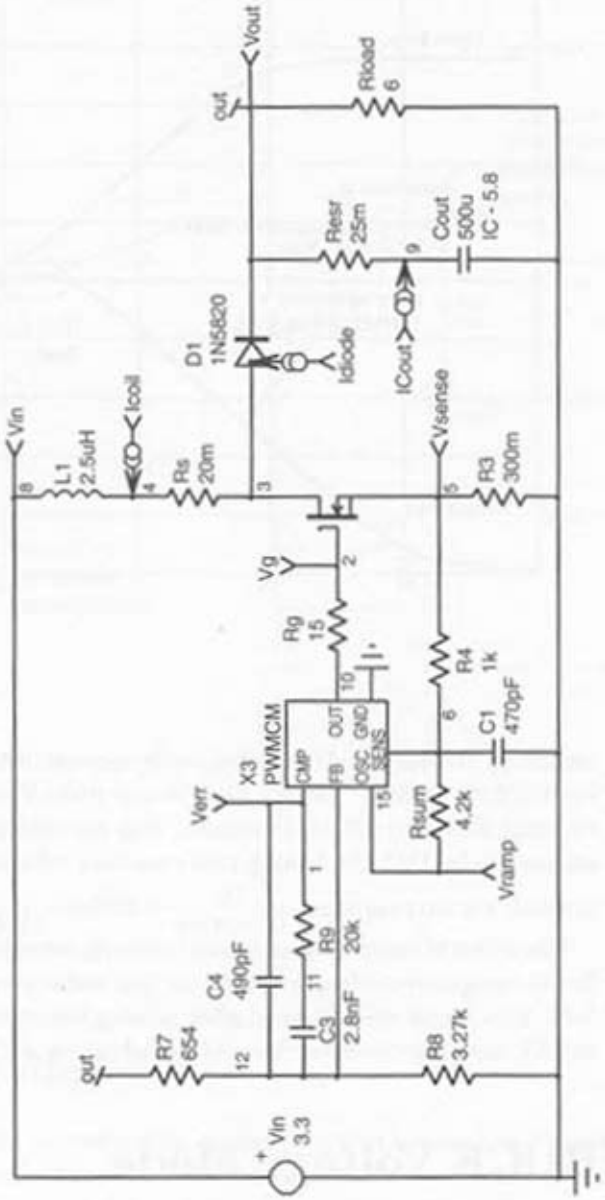


Figure 3-3e
The BOOST in current mode.

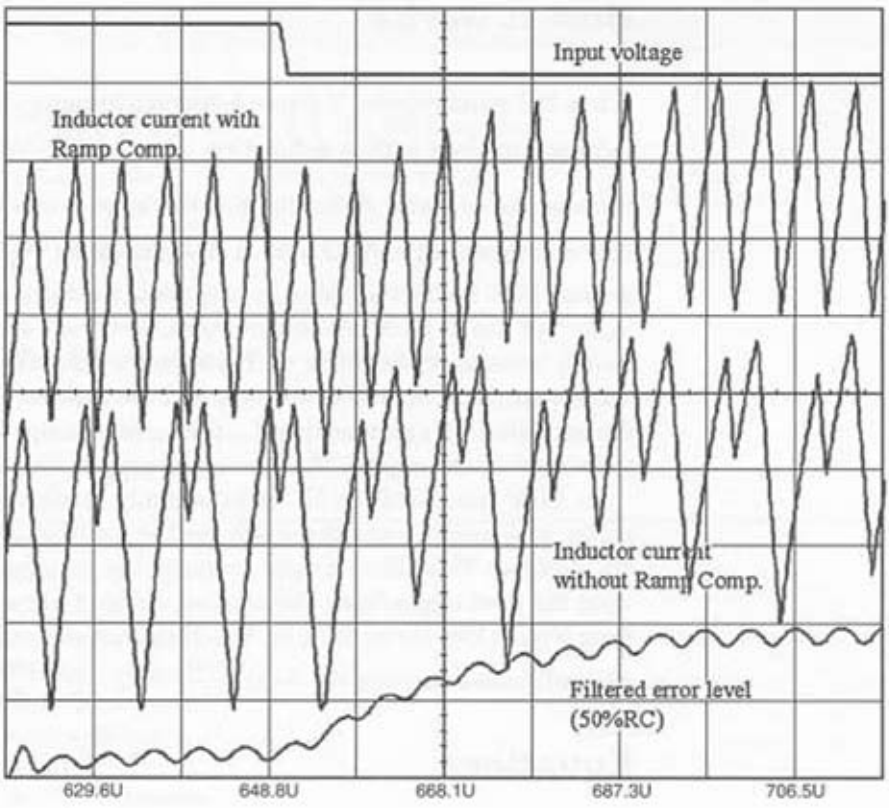


Figure 3-3f
Adequate ramp compensation stops subharmonic oscillations.

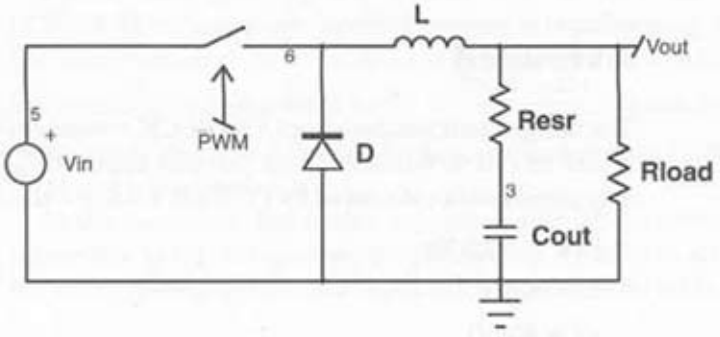


Figure 3-4a
A classical voltage-mode BUCK converter.

How It Works

When the switch closes, it forces a current to ramp-up in the inductor. The inductor up-slope is thus defined by: $\frac{Vin - Vout}{L}$. When the switch opens, because the inductor fights to keep the amps-turns constant, the current now circulates through D with a down-slope of: $\frac{Vout}{L}$. If the inductor is greater than its critical value L_C, the diode conducts until the switch closes again: we are in CCM. At this moment, a current spike takes place in the switch because of the diode t_{rr}. If you use a Schottky diode, there is no t_{rr} (except parasitic capacitive storage) and the problem greatly diminishes. At the opposite, if L is smaller than L_C, the current ramps down to zero and stays there until the next cycle. The previous diode problem is not present in DCM.

In CCM, the Vout/Vin DC gain is really straightforward. See the converter as a square-wave generator (on the junction of D and L) followed by an LC filter. This filter simply averages the square-wave signal and acts upon the final ripple level. The average value of a square-wave signal going from 0 up to Vin during D is: D . Vin. However, since the inductor is the seat of ohmic losses through *rlf*, then: $\frac{Vout}{Vin} = D \cdot \frac{Rload}{rlf + Rload}$.

Equations

Following are the equations for a voltage-mode control BUCK converter operating in CCM or DCM. These equations, as well as the ones later given, are a compilation of results found in references [15, 19, 20, 21] (See Table 3-4.)

Averaged

The design example depicts a CCM BUCK converter delivering 2.5V@1W to a DSP circuit as found in many portable applications (Vin = 2.7V to 4.8V). The parameters calculated by POWER 4-5-6 are the following:

Fsw = 200kHz

L = 60µH

rlf = 50mΩ

Cout = 220µF, 100mΩ ESR

Rload = 6.25Ω

Table 3-4

BUCK Voltage-Mode Equations.

	DCM	CCM
1st order pole	$\frac{2-M}{2\cdot\pi\cdot(1-M)\cdot Rload\cdot Cout}$	
2nd order pole	None because of DCM	$\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C_{out}}}$
Left Half-Plane Zero	$\frac{1}{2\cdot\pi\cdot R_{ESR}\cdot C_{out}}$	$\frac{1}{2\cdot\pi\cdot R_{ESR}\cdot C_{out}}$
Right Half-Plane Zero	—	—
V_{output}/V_{input} DC Gain	$\frac{2}{1+\sqrt{1+\frac{8\cdot\tau_L}{D^2}}}$	D
V_{output}/V_{error} DC Gain	$\frac{\sqrt{Vin\cdot(Vin-Vout)}}{\sqrt{2\cdot\tau_L}}$	Vin

F_{SW} = switching frequency
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
Cout = output capacitor
Vin = input voltage
Vout = output voltage
L = main inductor
D = duty-cycle
M = Vout/Vin conversion ratio
t_L = L / Rload . Tsw

Figure 3-4b portrays the typical way to wire the GSIM BUCK CCM/DCM voltage-mode model. However, it is interesting to confirm that the converter operates in CCM at high-line (4.8V, D = 0.52). By applying the critical inductance formula $Lc = \frac{R\cdot(1-D)}{2\cdot Fsw}$, we can determine if we really are CCM: Lc = 7.5µH (value under which we are DCM) << 60µH → CCM okay. (See Figure 3-4c.)

At the resonance, the double pole pushes the phase down to −180°. The higher the LC Q, the sharper the phase drop. Thanks to an adequate double zero positioning, the final bandwidth is still comfortable.

AVERAGE RESPONSE TO AN OUTPUT STEP One advantage of AC models is the lack of switching component. Thanks to this feature, transient simulations are performed in a snap and you can easily iterate the way you

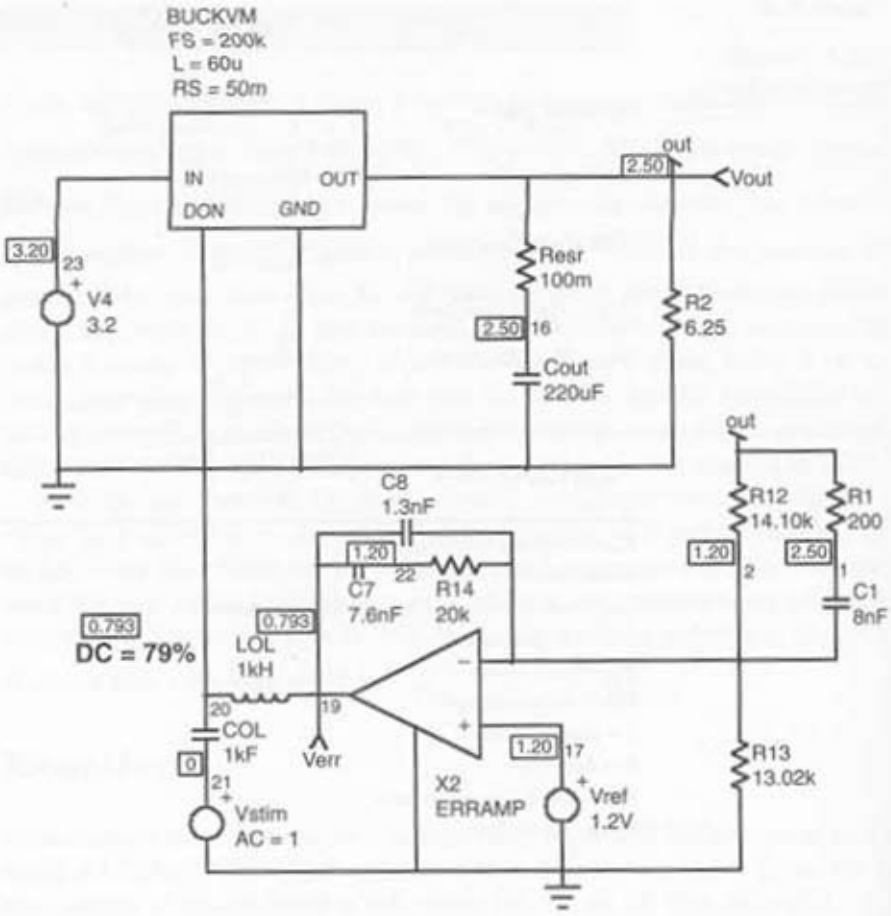


Figure 3-4b
The CCM BUCK converter simulation example.

finally shape your compensation error amplifier. Figure 3-4d details how to wire the varying output load; either a *Piece Wise Linear* (PWL) voltage source drives an ideal switch, or a PWL current source describes how the current step evolves with time:

```
V1 4 0 PWL 0 1 100u 1 100.1u 0 800u 0 800.1u 1
```

or

```
Istep out 0 PWM 0 400m 100u 400m 100.1u 80m 800u 80m 800.1u 400m
```

The result appears in Figure 3-4e. It shows an excellent transient response without excessive overshoot.

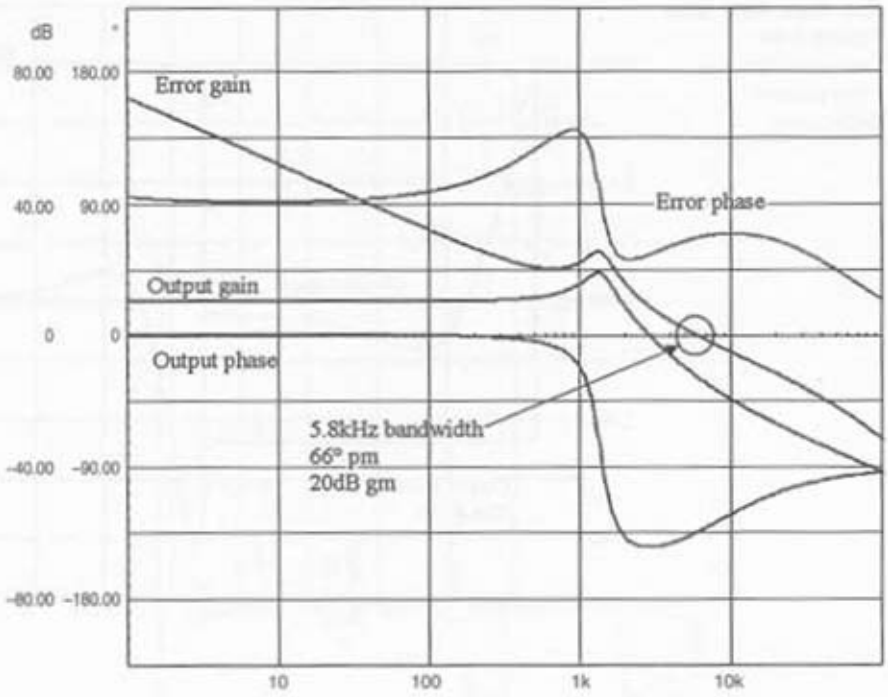


Figure 3-4c
The compensation network gives a 5.6kHz bandwidth with a good phase margin.

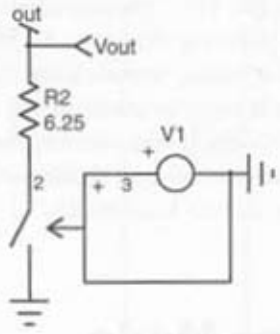


Figure 3-4d
A simple test fixture to perform an output step load.

Switched

The switched version uses our generic voltage-mode model already implemented in the BOOST section. We simulated Figure 3-4f example to be affected by the previous operating conditions.

The output was pulsed from 80mA up to 400mA. We selected a true N-channel MOSFET in the role of the switch. Thanks to the generic aspect of

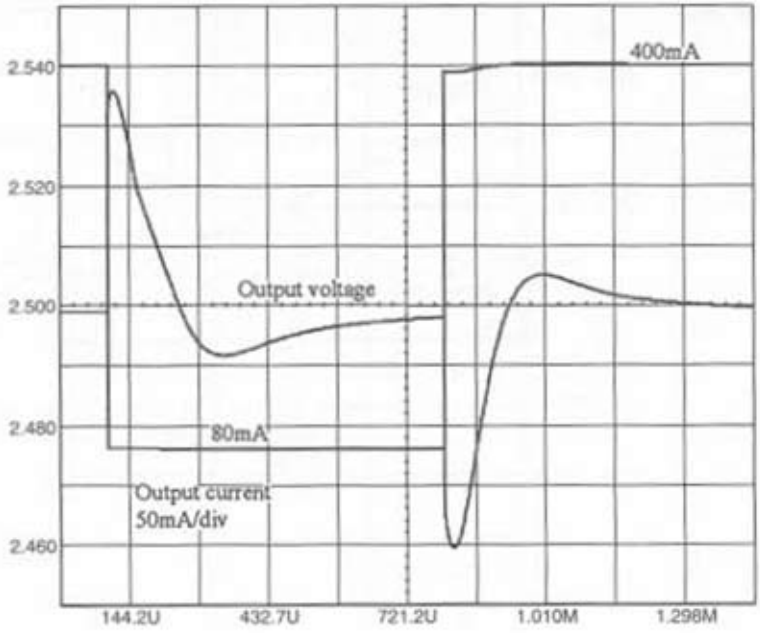


Figure 3-4e
The results show a 1.3% positive overshoot.

the controller, by changing the VOH parameter to 13V, we naturally produce a bootstrapped V_{GS} to properly drive the MOSFET (its source is floating). The result in Figure 3-4g nicely agrees with Figure 3-4e, except for the amplitude of the dip, which is more pronounced in our switched simulation due to the various series resistors not accounted for in the model. The reaction time of the loop when the load switch closes perfectly, sticks to the average model, implying similar circuit bandwidths.

BUCK Current Mode

The current-mode version of the BUCK does not differ much from the Figure 3-4a example; the sense primarily used for current protection now carries the instantaneous inductor current to the controller for the t_{ON} generation.

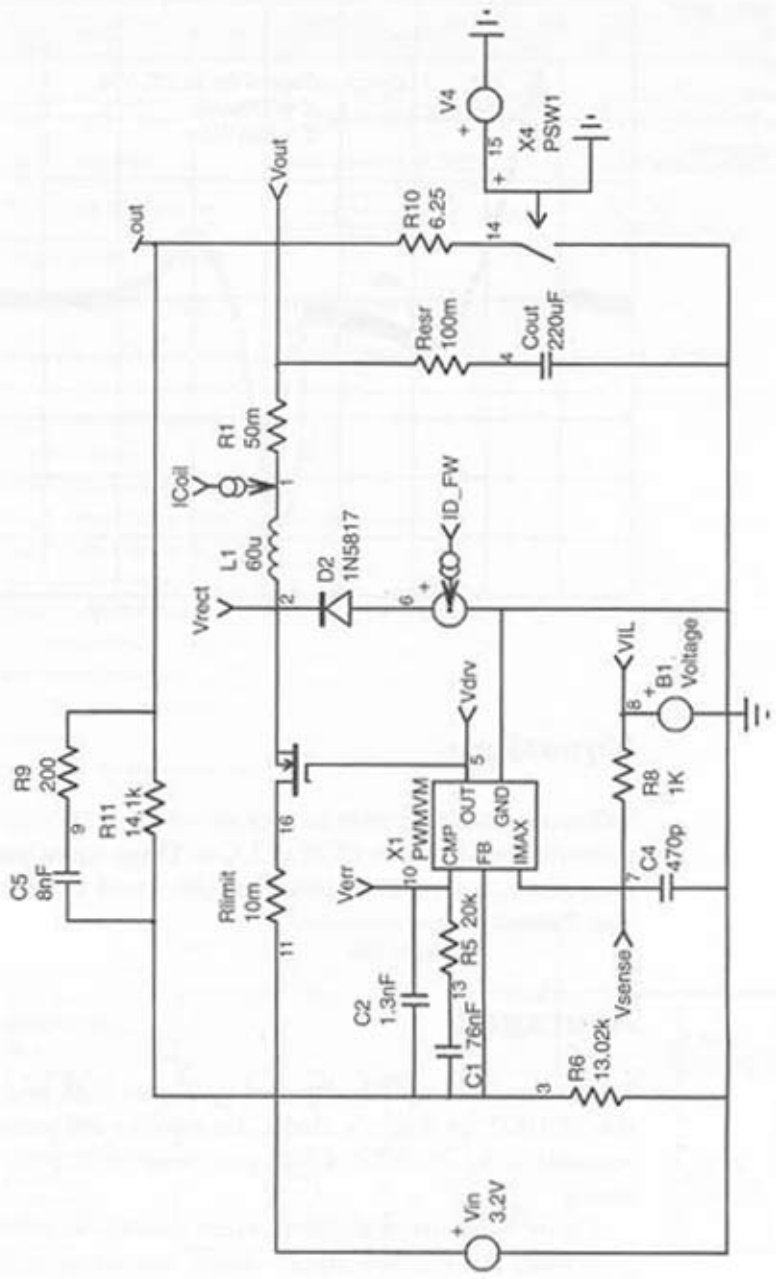


Figure 3-4f
The 200kHz voltage-mode BUCK converter.

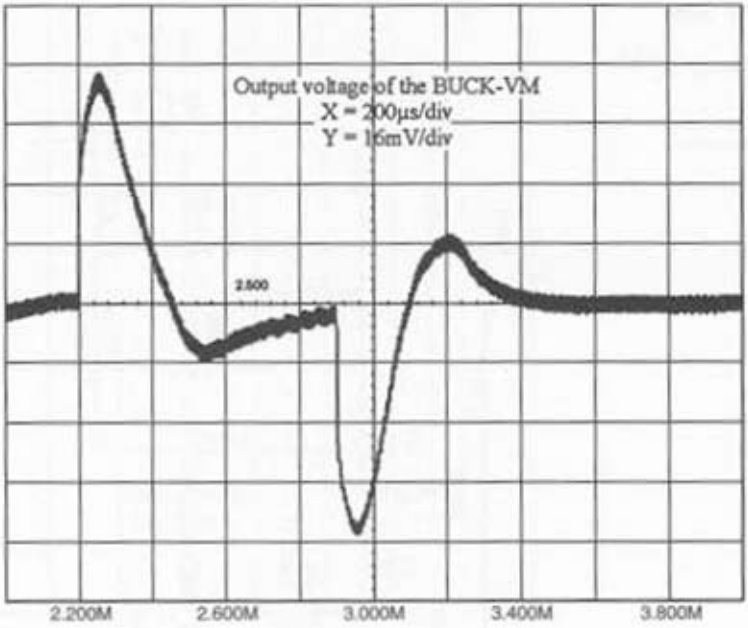


Figure 3-4g
The response to an output step reveals a small undercompensation.

Equations

Following are the first-order equations for a current-mode control BUCK converter operating in CCM or DCM. These equations, as well as the ones later given, are a compilation of results found in references [15, 19, 20, 21]. (See Table 3-5a.)

Averaged

The average example is depicted by Figure 3-4h where you now recognize the BUCKCCM Ridley's model. By passing the parameters calculated by yourself or by POWER 4-5-6, you directly observe the variable of your choice.

Figure 3-4i unveils the simulation results. As you can see, the open-loop gain looks good at low-input voltage, but when you reach the maximum value, the subharmonic poles suddenly pull the gain plot above the zero dB axis and could jeopardize your stability. Increasing Mc to 1.5 will provide 50 percent compensation ramp, and our problem fades away.

Table 3-5a

BUCK Current-Mode Equations

	DCM	CCM
1st-order pole	$\frac{2-M}{2\cdot\pi\cdot(1-M)\cdot Rload\cdot Cout}$	$\frac{1}{2\cdot\pi\cdot Rload\cdot Cout}$
2nd-order pole	None because of DCM	None because of CM
Left Half-Plane Zero	$\frac{1}{2\cdot\pi\cdot R_{ESR}\cdot C_{out}}$	$\frac{1}{2\cdot\pi\cdot R_{ESR}\cdot C_{out}}$
Right Half-Plane Zero	—	—
V_{output}/V_{input} DC Gain	see reference [21]	D
V_{output}/V_{error} DC Gain	see reference [21]	$k\cdot Rload$

F_{SW} = switching frequency
D = duty-cycle
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
C_{OUT} = output capacitor
Vin = input voltage
Vout = output voltage
L = main inductor
Vc = control voltage
k = max. Ipeak/max. Vc
Ipeak = k · Vc
M = Vout/Vin conversion ratio

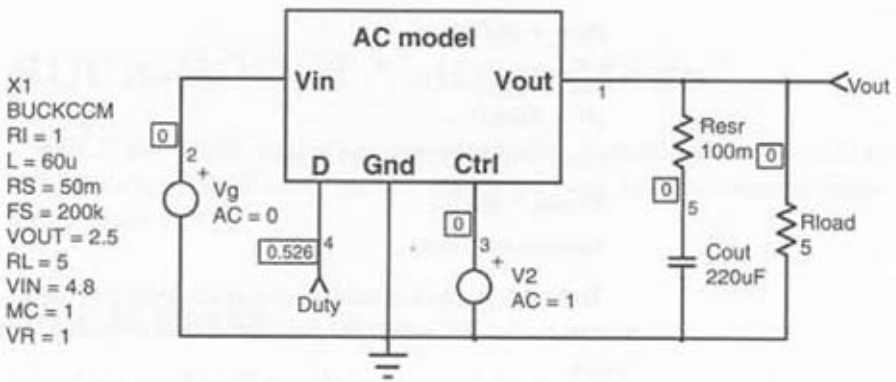


Figure 3-4h
The BUCK CCM model for continuous simulations.

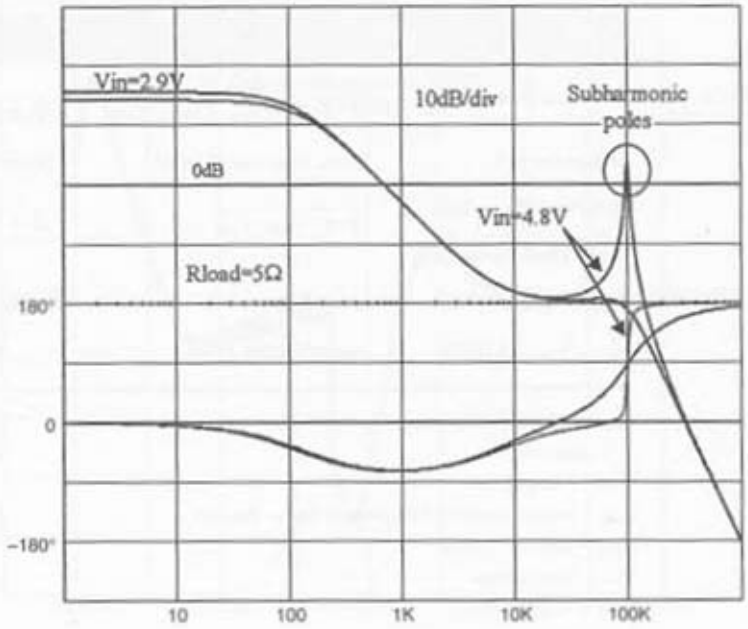


Figure 3-4i
When increasing Vin, the subharmonic poles start to peak.

Switched

Our CM design example depicts the same CCM BUCK converter, which still delivers 2.5V@1W. The following parameters are summarized where a sense element has been added:

Fsw = 200kHz

L = 60µH

rlf = 50mΩ

Cout = 220µF, 100mΩ ESR

Rload = 6.25Ω

Rsense = 10mΩ

To compensate for subharmonic oscillations, we need to inject a compensation ramp. We select 50 percent of the inductor downslope: 50 percent of $\frac{Vout}{L}$ = 20.8mA/µs or 104mA/5µs. With an Rsense of 10mΩ, we would obtain a final level of 1.041mV, a bit difficult to produce when compared to the ambient noise. Thanks to an amplifier gain of 100, we raise our current

level to 104.1mV. From a 5V ramp voltage, we shall then divide by a factor of 4.8. If the current information is carried via a 1kΩ resistor, the 5V ramp will thus be applied through a 48kΩ.

Figure 3-4j differs from the previous applications because we added the dead-time generator to perform synchronous rectification. To comply with a P-MOS type, you need to add an inverter in series with a generic model. The dead-time allows the elimination of the shoot-through (also called cross-conduction) between the MOSFETs. We selected a 200ns value. The Figure 3-4f system gave an efficiency of 93.5 percent. By the way, to calculate the input power (in Watts) for *any waveforms,* follow the steps once SPICE has terminated its simulation:

1. Display the input current I(t) and the voltage V(t) of the input source (in our case, V(t) is constant to 3.2V).
2. Multiply both curves together.
3. Take the average of the results: you obtain Watts. With Vin constant, simply get the average input current and multiply by Vin.

After simulation, Figure 3-4h delivers an efficiency of 95.1 percent. Figure 3-4k depicts some typical waveforms. As you can see, at the switch turn-off, the free-wheel diode immediately takes over before the N-channel MOSFET (due to the 200ns dead-time). However, because of the CCM operation, this free-wheel diode conducts again just before the main P-channel MOSFET turns on. When this main series switch applies Vin to node 2, it brutally forces the diode to stop conducting. Figure 3-4k clearly depicts the resulting current spikes that occur in the switch until the diode is finally blocked.

BUCK-BOOST Voltage Mode

The BUCK-BOOST converter is presented in Figure 3-5a. As usual, for rugged voltage-mode designs, pulse-by-pulse peak inductor current monitoring is advised.

How It Works

When the switch closes, it forces a current to ramp-up in the inductor according to the formula: $\frac{Vin}{L}$. When the switch opens, the inductor fights

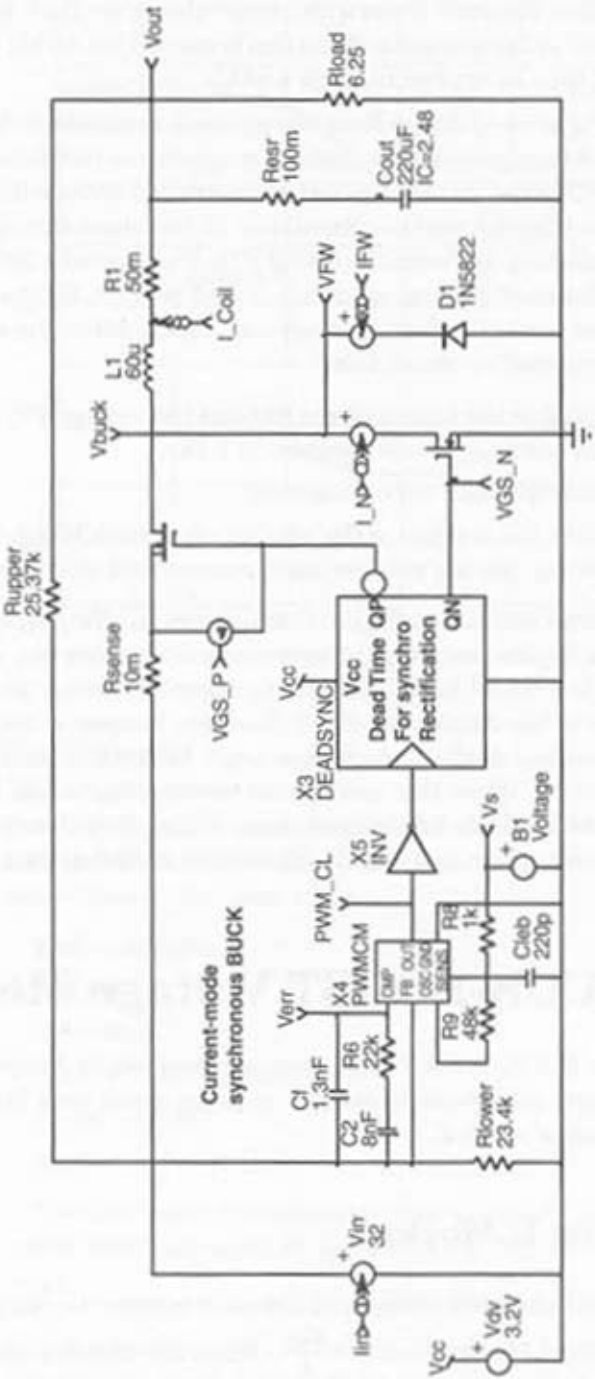


Figure 3-4j
This application makes use of the dead-time generator to avoid any shoot-through currents.

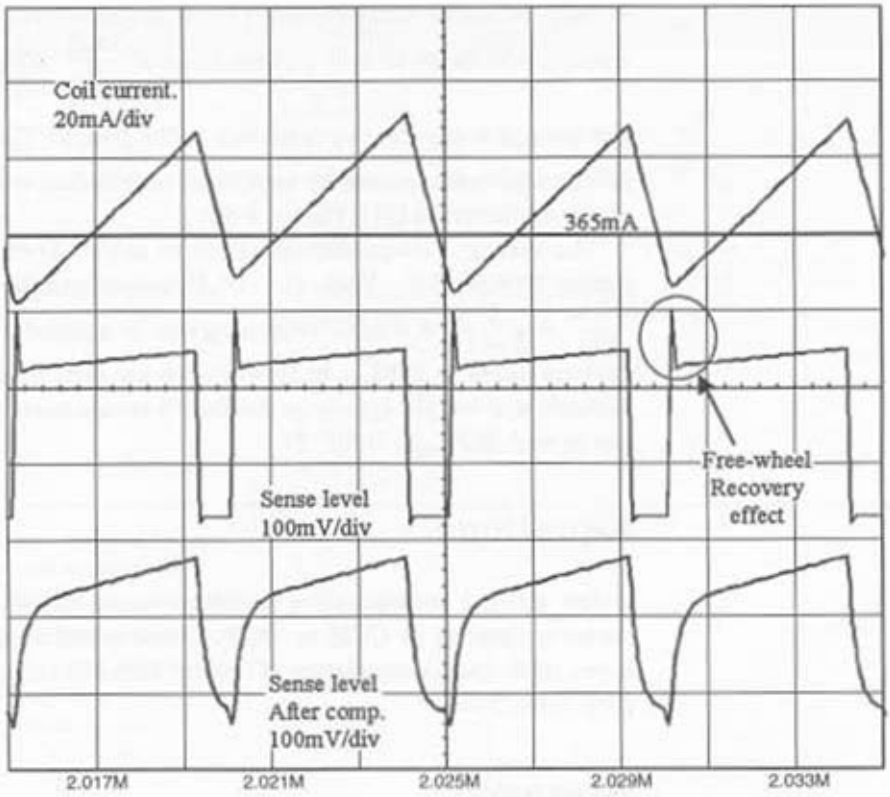


Figure 3-4k
Some typical waveforms of the BUCK current mode.

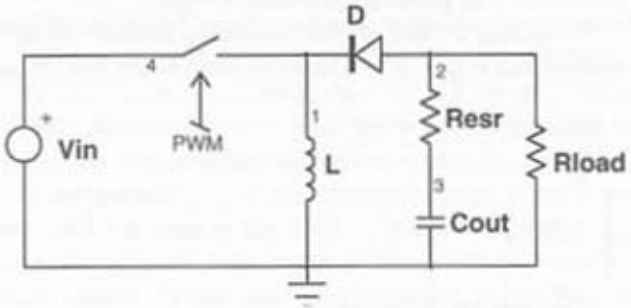


Figure 3-5a
A classical voltage-mode BUCK-BOOST converter

to keep the amps-turns constant by reversing its voltage. The current now circulates through D with a down-slope of $\frac{Vout}{L}$. Please note that the output voltage is negative by reference to the ground. The $\frac{Vout}{Vin}$ transfer ratio is found instantaneously by applying the inductor voltage-balance reached at the equilibrium [21] (Figure 3-5b).

The average voltage during switch-on is Vin · D and the average voltage during switch-off is −Vout · (1 − D). By equating both equations, you obtain $\frac{Vout}{Vin} = \frac{D}{1-D}$. A similar reasoning can be applied if one wants to include various losses as $RDS_{(ON)}$ or forward voltage drop Vf, and so on. These components will simply appear in the final formula averaged over their operating period: $RDS_{(ON)}$ · D, Vf · D'.

Equations

Below are the equations for a voltage-mode control BUCK-BOOST converter operating in CCM or DCM. These equations, as well as the ones given later, are a compilation of results found in references [15, 19, 20, 21]. (See Table 3-5b.)

Averaged

One of the biggest interests of averaged models lies in the prediction of poles (or zeroes) that move in function of the duty-cycle in CCM. Iterations by hand to properly stabilize the system could easily take hours. Fortunately, SPICE picks off the cases for us.

To change a little, we have selected Ridley's model FLYBACKCCM. This component requires you to enter the values you (or an automated software)

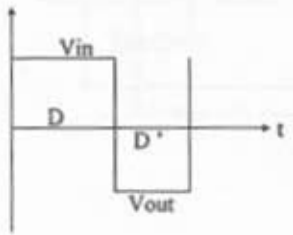


Figure 3-5b
By equating both areas, you easily deduct the DC transfer function.

Table 3-5b

BUCK-BOOST Voltage-Mode Equations.

	DCM	CCM
1st-order pole	$\frac{1}{\pi \cdot R_{load} \cdot C_{out}}$	
2nd-order pole	High frequency pole, see reference [5, 21]	$\frac{(1-D)}{2 \cdot \pi \cdot \sqrt{L \cdot C_{out}}}$
Left Half-Plane Zero	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [5, 21]	$\frac{R_{load} \cdot (1-D)^2}{2 \cdot \pi \cdot L \cdot D}$
V_{output}/V_{input} DC Gain	$D \cdot \sqrt{\frac{R_{load}}{2 \cdot L \cdot F_{SW}}}$	$\frac{D}{(1-D)}$
V_{output}/V_{error} DC Gain	$Vin \times \sqrt{\frac{R_{load}}{2 \cdot L \cdot F_{SW}}}$	$\frac{Vin}{(1-D)^2}$

F_{SW} = switching frequency
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
Cout = output capacitor
Vin = input voltage
Vout = output voltage
L = main inductor
D = duty-cycle

calculated. Lsec is the nominal inductance value, Ri is put to zero because of voltage-mode control, and finally, Vr details the PWM sawtooth amplitude (the actual PWM modulator gain). Put this parameter to 1 if you do not know this. The simulation file appears in Figure 3-5c.

Our example delivers −8V@10A from a car battery. Its minimum level is 10V. The output capacitor is affected by an *Equivalent Series Resistor* (ESR). If our converter evolves in an automotive environment, the surrounding temperature is likely to change. As a result, the ESR grows up to low temperatures but decreases to higher levels. How does it affect the stability? By sweeping the ESR parameter from the min/max numbers given by the capacitor data-sheet, Figure 3-5d tells you how the control/output gain moves. In our case, the variation is not too stringent, but it clearly identifies the ESR as a potential stability "killer" if you do not account for it at the design stage. It also demonstrates the ease of a parameter iteration with SPICE.

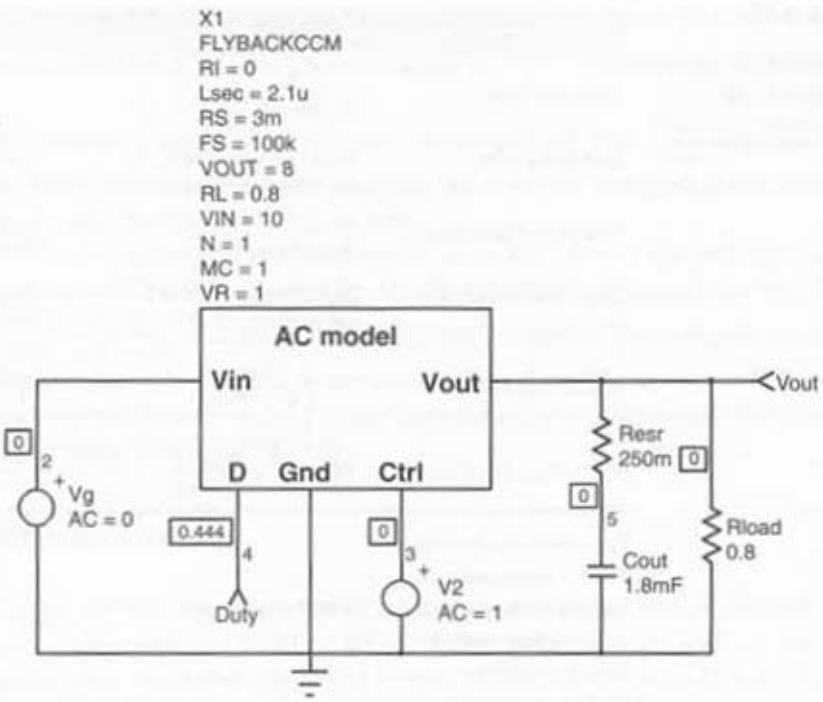


Figure 3-5c
CCM BUCK-BOOST simulation file

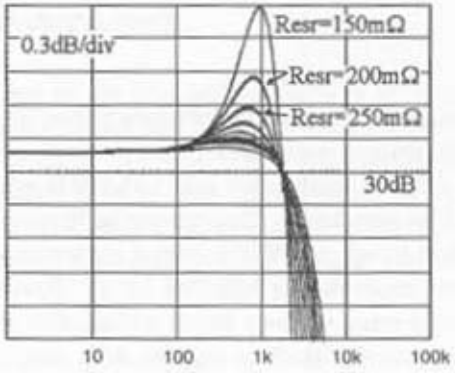
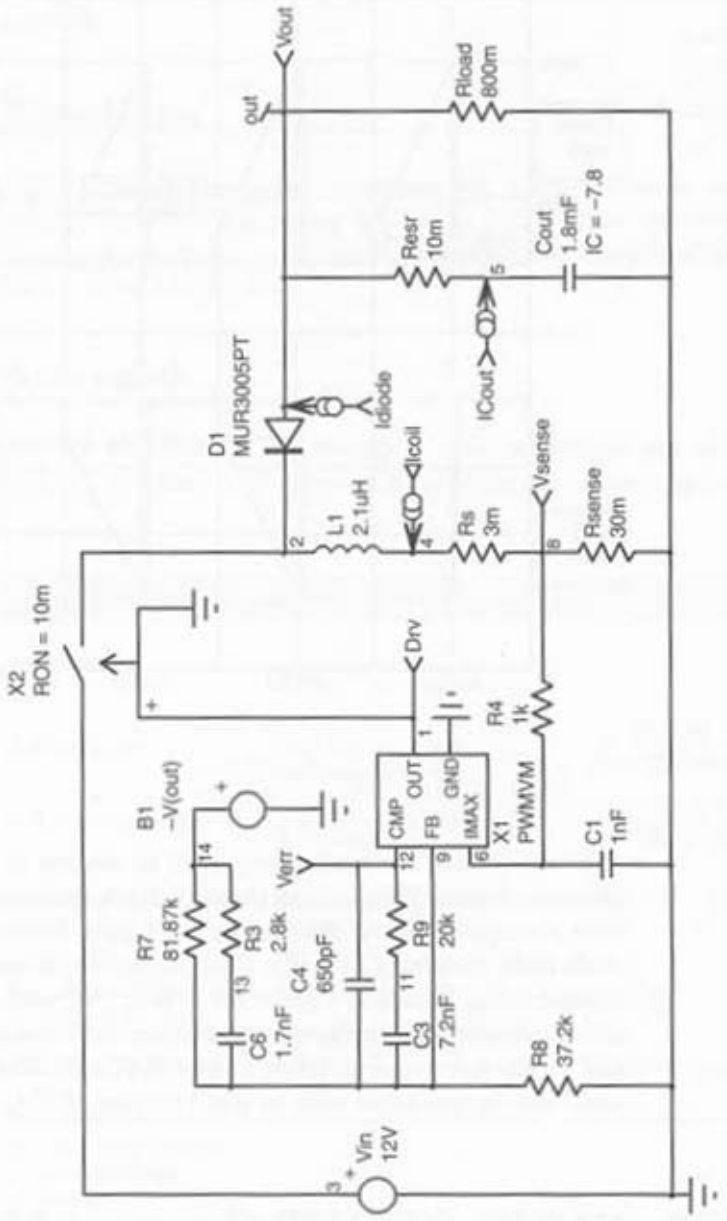


Figure 3-5d
ESRs variation (with temp or age) acts upon the final shape.

Switched

The switched version uses the generic voltage-mode model, already implemented in the BUCK section. We simulated the Figure 3-5e example: a neg-

Figure 3-5e
The BUCK-BOOST switched version requires a slight modification.



ative 80W inverter. The P-MOSFET has been replaced by a generic switch affected by a 10mΩ conduction resistance. (See Figure 3-5f.)

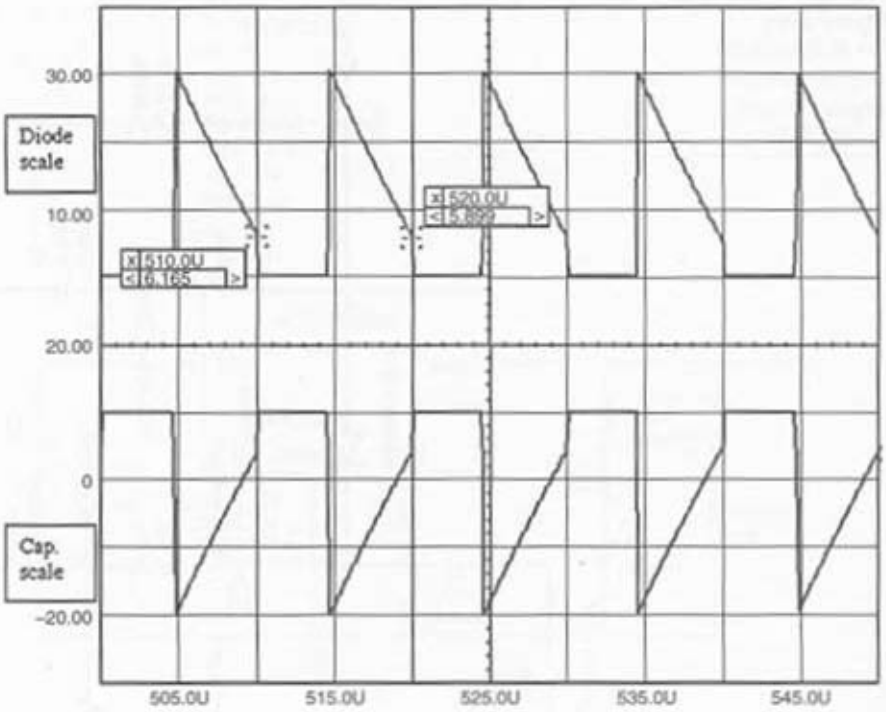


Figure 3-5f
Operation reveals a high diode RMS current of 14A.

Because Vout is negative, we need to inverse it to satisfy the generic implementation. This is done through B1, a B element. It could also have been a simple E source affected by a −1 gain. Simulation results reveal a diode RMS current of 14A. The total conduction losses can therefore be calculated using Pdiode = I^2rms · Rd + Iavg · Vf, with Rd the dynamic (also called incremental) diode resistance taken from the data-sheet at Id = 14A and Vf, the forward drop taken at Id = 9A (Iavg). The capacitor dissipation could also be extracted with an RMS current of 10A: I^2rms · ESR.

BUCK-BOOST Current Mode

The current-mode version does not differ much from the voltage-mode. Compared to Figure 3-5e, the Vsense information will be routed to the sense

comparator to end the switch on-state when the correct Ipeak value is reached.

Equations

Below are the first-order equations for a current-mode control BUCK-BOOST converter operating in CCM or DCM. These equations, as well as the ones later given, are a compilation of results found in references [15, 19, 20, 21]. (See Table 3-6.)

Averaged

INPUT IMPEDANCE Switched-mode converters are inherently noisy and can interfere with equipment sharing the same supply lines. This is

Table 3-6

BUCK-BOOST Current-Mode Equations.

	DCM	CCM
1st-order pole	$\frac{1}{\pi \cdot R_{load} \cdot C_{out}}$	
2nd-order pole	High frequency pole, see reference [5, 21]	$\frac{(1+D)}{2 \cdot \pi \cdot C_{out} \cdot Rload}$
Left Half-Plane Zero	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [5, 21]	$\frac{R_{load} \cdot (1-D)^2}{2 \cdot \pi \cdot L \cdot D}$
V_{output}/V_{input} DC Gain	$k \cdot Vc \cdot \sqrt{\frac{Rload \cdot L \cdot Fsw}{2}}$	$\frac{D}{(1-D)}$
V_{output}/V_{error} DC Gain	$k \cdot \sqrt{\frac{Rload \cdot L \cdot Fsw}{2}}$	$k \cdot Rload \cdot \frac{Vin}{2 \cdot Vout + Vin}$

F_{sw} = switching frequency
L = main inductance
D = duty-cycle
Cout = output capacitor
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
Ipeak = k · Vc
k = max. Ipeak/max. Vc
Vc = error voltage

particularly true in automotive applications. To prevent disturbances from being routed via these lines, you need to install a specific filter in front of your converter. Most of the time, this *ElectroMagnetic Interference* (EMI) filter will be reactive. The problem comes from the nature of the load applied to the filter output: the converter's input. Let's take a closer look. In a closed-loop system, the loop strives to maintain a constant output power regardless of operating conditions. If you insert an Ampmeter in series with your converter and modulate the input line, you will see that if Vin grows, the input current diminishes (this makes sense, the supply strives to keep Pout constant), while a drop of Vin is followed by an increase of Iin. From this input side, the converter looks like a negative resistor! Watch for the lines.

We can write the following equations, assuming we have a 100% efficiency:

$$\text{Pin} = \text{Pout} = \text{Iin} \cdot \text{Vin} = \text{Iout} \cdot \text{Vout}$$

$\rightarrow \frac{Vin}{Vout} = \frac{Iout}{Iin} = \mu$, the conversion ratio. Now, since $Zin = \frac{Vin}{Iin}$ then the *incremental* impedance can be found by calculating $\frac{dVin}{dIin}$. Vin can be expressed by $\frac{Pin}{Iin}$ but since Pin = Pout = Rload · Iout^2, then the final equation becomes: $\frac{dVin}{dIin} = \frac{d}{dIin}\frac{Rload \cdot Iout^2}{Iin}$ and leads to: $-Rload \cdot \frac{Iout^2}{Iin^2} = -Rload \cdot \mu^2$ a negative number.

It is important to assess the boundaries of this input impedance Z_{in}. Why? Because if your negative incremental resistance compensates for the filter ohmic losses, you cancel any resistive damper that normally stops the eventual transient LC oscillations: you have built a *Negative Impedance Converter* (NIC) oscillator. Thanks to average models, SPICE evaluates the input impedance in the easiest way. Figure 3-5g details how to wire RIDLEY's model.

The results are displayed in Figure 3-5h, and detail how Z_{in} moves with different ramp compensation levels. The static portion is found by calculating the input current for the considered converter (η = 100%): Iin = Pout/Vin or 8A. Zin is then evaluated at 1.25Ω or 1.93dBΩ. A comprehensive simulation exercise would also include output impedance Z_{out} plots of the front-end filter you designed. To avoid any conflict between your filter and this converter, you would check that no overlap area ever exists between Z_{in} and Z_{out}. In other words, you shall keep the input impedance Z_{in}

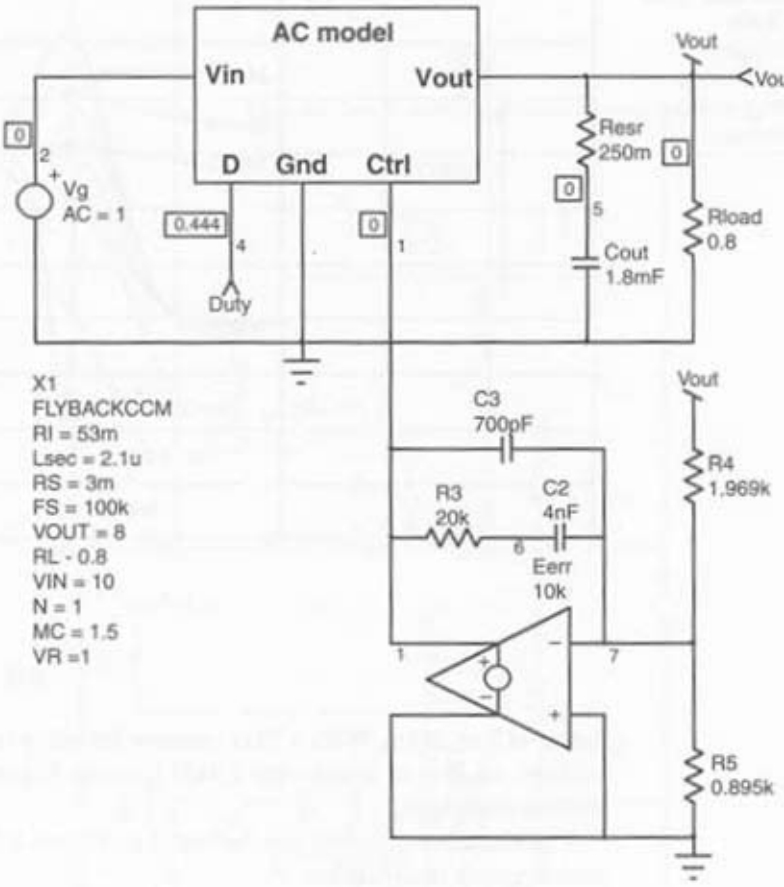


Figure 3-5g
By monitoring the Vg/Iin ratio, you can plot the input impedance.

well above the filter's output impedance Z_{out}. Otherwise, a conflict might occur.

Switched

The switched simulation is simply the current-mode version of the Figure 3-5e example. Because of CCM, we need to compensate for subharmonic oscillations. The inductor downslope is Vout / L or 38A/10µs. Fifty percent of it reflected on Rsense gives a necessary ramp amplitude of 1V. From our 5V level given by the generic model, we need to divide by a

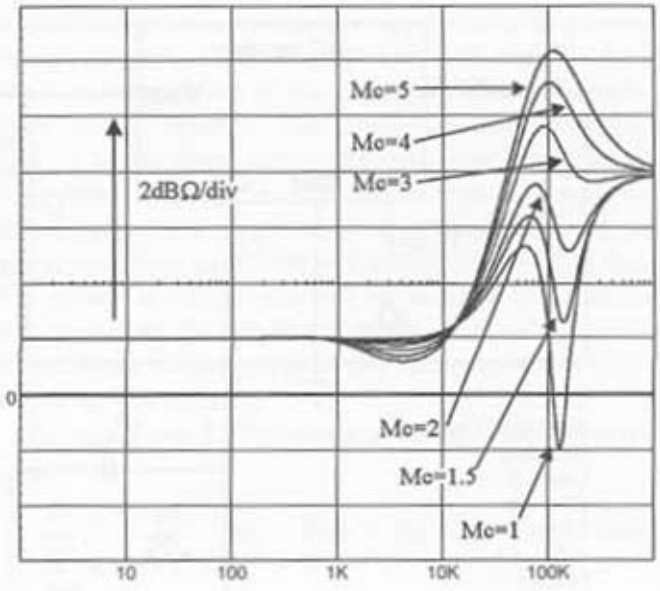


Figure 3-5h
Various input impedance results depending on slope compensation.

factor of 5 or 201m. With a 1kΩ resistor bringing the current sense information, we should inject with a 4kΩ resistor. Figure 3-5i details the simulation template.

The simulation results are delivered in Figure 3-5j and do not show any subharmonic instabilities.

FLYBACK Voltage Mode

The FLYBACK converter is presented in Figure 3-6a. It is probably one of the most popular topologies found in many low- and medium-power applications such as offline battery chargers, wall packs, and so on. Years ago, the majority of designs built around the popular SG1524 circuits did not include pulse-by-pulse current limitation. Fortunately, nowadays, circuits like the MC44608 from *ON Semiconductor* (Phoenix, AZ) let you build rugged voltage-mode SMPS by including fast overcurrent detection.

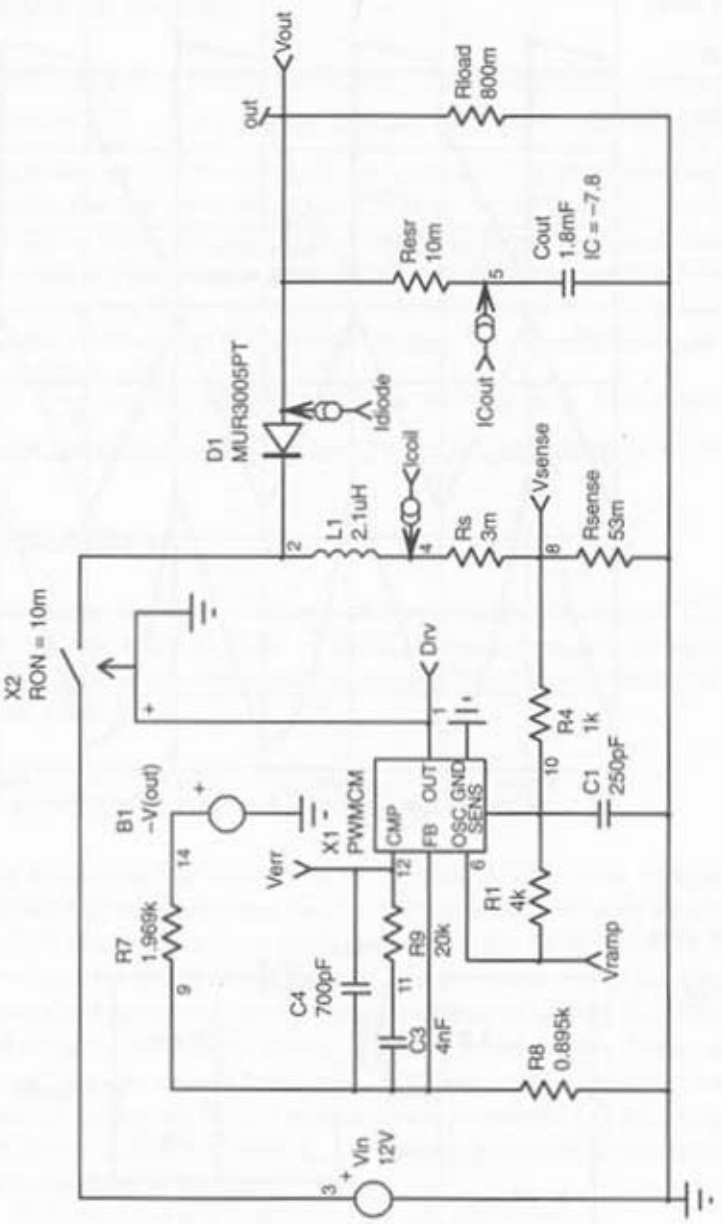


Figure 3-5i
The current-mode implementation of the BUCK-BOOST converter

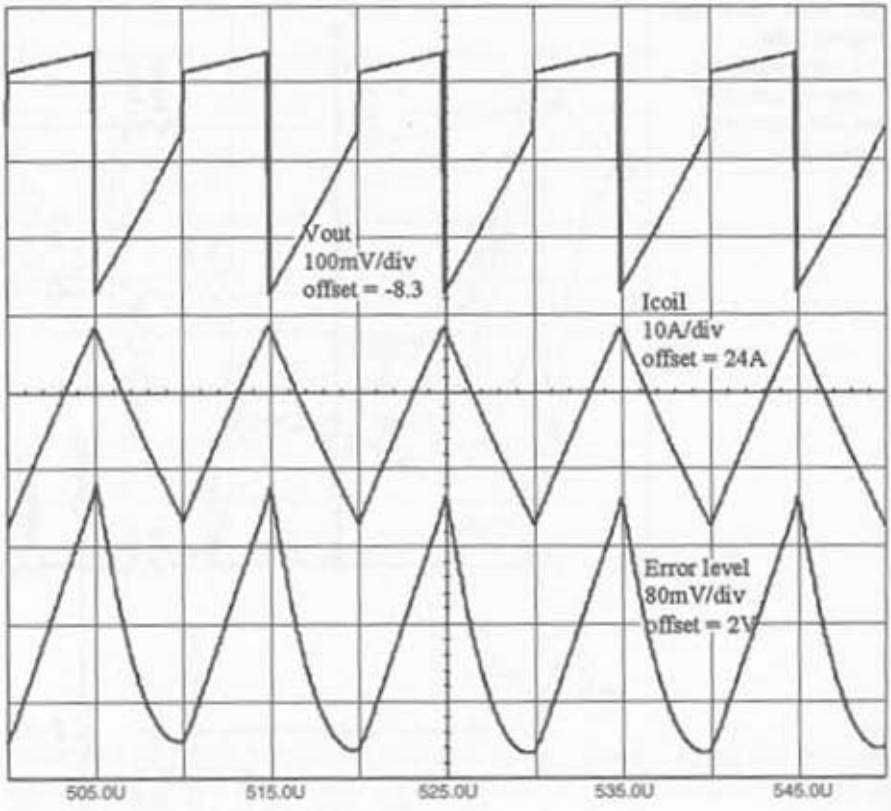


Figure 3-5j
Simulation results reveal a large inductance ripple.

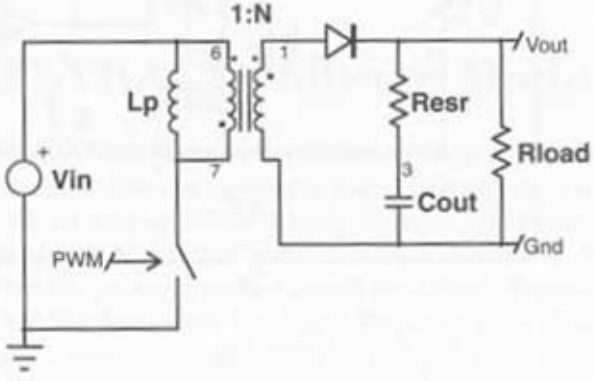


Figure 3-6a
A simplified FLYBACK converter highlighting the presence of the magnetizing inductance.

How It Works

When the power switch closes, the current in primary ramps-up at a rate given by $\frac{Vin}{Lp}$, with Lp as the primary inductance, also called the magnetizing inductance. Because of the diode, no current circulates in the secondary during the ON time. When the PWM dictates the switch opening, the core magnetic field collapses. In an attempt to keep the amps-turns circulating, the primary inductance reverses its voltage; D can now conduct and the primary current finds a way to circulate through Cout but also Rload. The ramp-down current is therefore imposed by the reflected Vout voltage over Lp: $\frac{(Vout + Vf)}{Lp \cdot N}$, with Vf the diode forward drop. By adjusting the duty-cycle, the circuit is able to regulate the output voltage at the desired level.

Equations

Following are the equations for a voltage-mode control FLYBACK converter operating in CCM or DCM. These equations, as well as the ones given later, are a compilation of results found in references [15, 19, 20, 21]. (See Table 3-7.)

Averaged Low-Cost Feedback

We will draw the Bode plot of a DCM AC/DC wall adapter delivering 12V@1A from a universal mains (85 to 285VAC). Why do we purposely force DCM? Most of the time, designers select the DCM mode at high line but accepts to go CCM at low line. DCM represents a good solution at medium power, but as soon as the output power demand grows, the RMS current circulating in the output power capacitors and in the diode, becomes very large. But one salient feature of DCM lies in the absence of turn-on losses, usually generated by the output diode recovery in CCM. However, despite DCM and the lack of diode t_{rr}, the various parasitic capacitances contribute to some turn-on losses.

Following are the component values calculated:

Fsw:	100kHz
Lp:	2mH
1:N	1:0.0538
Cout:	470µF, Resr = 55mΩ

Table 3-7

FLYBACK Voltage-Mode Equations.

	DCM	CCM
1st-order pole	$\frac{1}{\pi \cdot R_{load} \cdot C_{out}}$	
2nd-order pole	High frequency pole, see reference [5, 21]	$\frac{(1-D)}{2 \cdot \pi \cdot \sqrt{Lsec \cdot C_{out}}}$
Left Half-Plane Zero	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [5, 21]	$\frac{R_{load} \cdot (1-D)^2}{2 \cdot \pi \cdot Lsec \cdot D}$
V_{output}/V_{input} DC Gain	$N \cdot D \cdot \sqrt{\frac{R_{load}}{2 \cdot Lsec \cdot Fsw}}$	$\frac{D}{(1-D)} \cdot N$
V_{output}/V_{error} DC Gain	$V_{in} \cdot N \cdot \sqrt{\frac{R_{load}}{2 \cdot Lsec \cdot Fsw}}$	$\frac{Vin}{(1-D)^2} \cdot N$

F_{sw} = switching frequency
Rload = output load
R_{ESR} = output capacitor's Equivalent Series Resistor
Cout = output capacitor
Vin = input voltage
Vout = output voltage
Lsec = secondary inductor = Lp · N^2
D = duty-cycle
Transformer ratio, 1 : N = Np:Ns

Figure 3-6b shows the complete SPICE FLYBACK simulation template using the GSIM model. The L parameter corresponds to the primary inductance value. This template includes a simplified feedback chain around an optocoupler and zener diode. We also add the PWM gain that you calculate knowing the sawtooth amplitude of the controller you have selected:

$G_{PWM} = \frac{1}{Vsaw}$ · (Vsaw = 2.5V in our example)

As you can see on the simulation schematic, the reflected DC levels indicate a good operating point: $V_{R3} + V_ZD1 + V_{be}X3$. The duty-cycle establishes at 60 percent for a 120V input voltage. The Bode plot appears on Figure 3-6c. With this kind of simplified feedback loop, there is not much flexibility to tailor the error amplifier section, since there is no error amplifier! The DC gain of this chain is given by R3 and R4: $\frac{R4}{R3} \cdot CTR$, with CTR the optocoupler CTR.

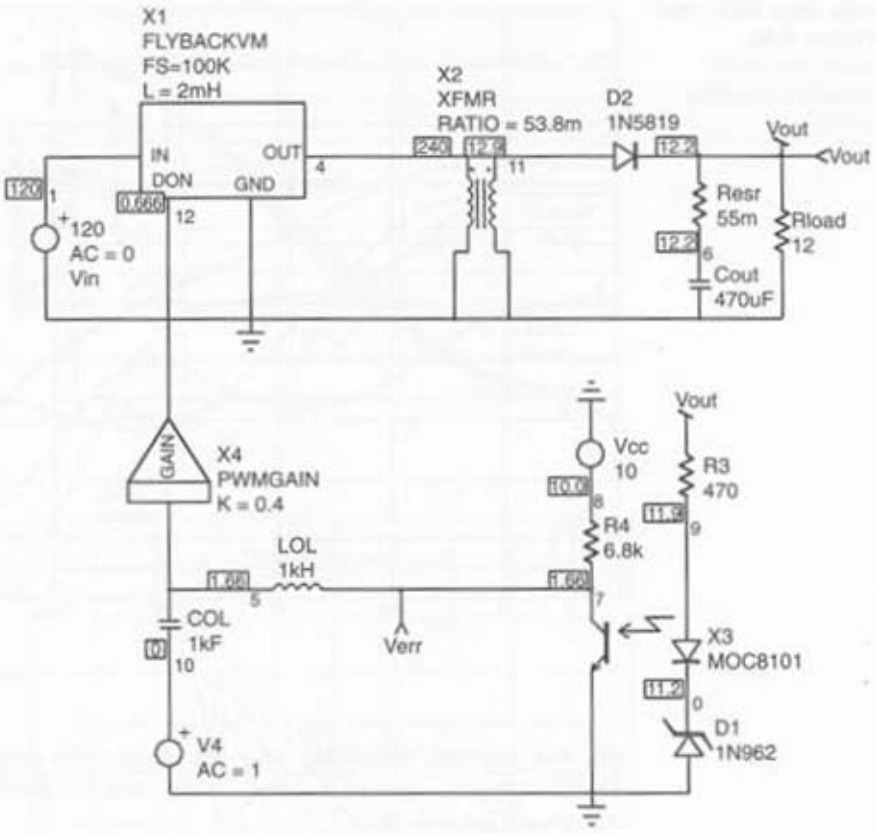


Figure 3-6b
A standard AC/DC converter using a low-cost feedback chain.

Averaged, Shunt Regulators

Classical PWM modulators generate a duty-cycle by comparing an error voltage to a ramp, but a new generation of PWM controllers emerged a few years ago. These new devices appear to be true monolithic circuits where the designers pushed everything inside the die: the PWM generation, the various protections, and sometimes the main power MOSFET. In these components, the duty-cycle is generated by forcing a current into a dedicated *feedback pin* (FB); this concept is called the shunt regulator: this is because you need to elevate the FB level until it is clipped to a regulation-level Vz at which the current starts to circulate. It is as if a zener were connected behind the FB pin; below the breakdown, a weak current flows and the duty-cycle equals the maximum value. As soon as you reach the thresh-

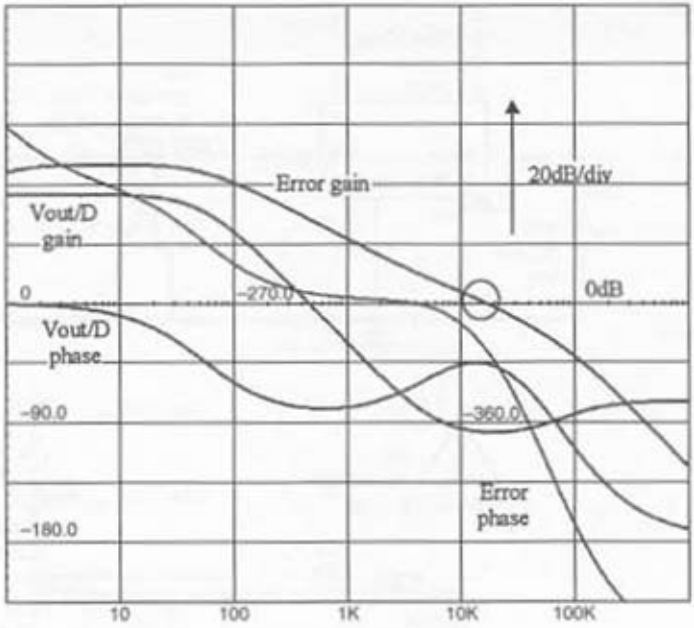


Figure 3-6c
Bode plot of the simplified feedback system.

old, the current circulates and the duty-cycle diminishes. Figure 3-7a depicts a typical variation curve for the new ON Semiconductor MC44608. (Also see Figure 3-7b.)

The way this modulator is built appears in Figure 3-7c, where the main P-channel MOSFET acts as variable resistor and deviates the FB current through ground. The current to duty-cycle conversion is done with Rgain whose value depends on the PWM function you target (actually given the product data-sheet). Finally, by adjusting the B1 component (or E1 in PSpice), you bound the duty-cycle to any value.

A Multioutput Shunt Regulator Example The MC44608 is an eight-pin voltage-mode PWM controller whose feedback implements a shunt regulator with a clipping voltage of typically 5V. Figure 3-7d portrays the open-loop configuration we have tested.

This is the opportunity to discover the power of SPICE in this kind of multioutput power-supply. In this monitor or TV application, the MC44608 is modeled with its duty-cycle shunt regulator. The duty-cycle generated from the opto-isolator is translated into voltage and directly feeds the average FLYBACK model. As you can see, the reflected DC points indicate a

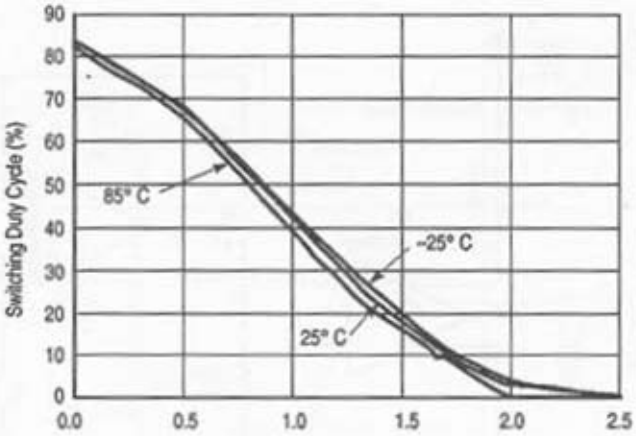


Figure 3-7a
When some current circulates through FB, D diminishes.

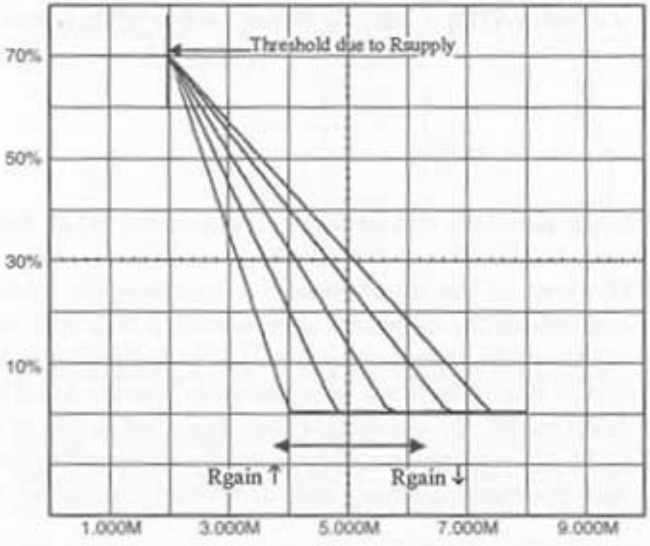


Figure 3-7b
A few components are required to tailor this curve.

clipping voltage of 5V, compatible with the data-sheet specs (node 16). In a normal Bode plot paper study, you would reflect all the load resistances, ESRs, and output capacitors (according to the respective turn ratios squared) to the main regulating point. SPICE does it automatically and includes the diode *incremental* resistor. What is that? When you carry your paper study, you simply reflect all the output elements as if they were connected to the transformer's secondary; this is the common mistake. Do not

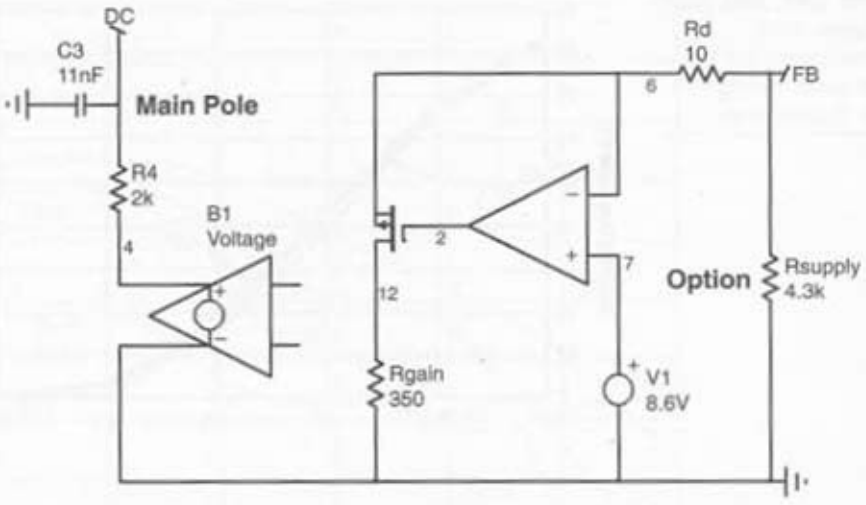


Figure 3-7c
The SPICE implementation of the PWM modulator—B1 bounds the DC between 70 percent and 0.2 percent.

forget the diode and its dynamic resistance Rd at the given operating current. At high output current, Rd is small and you can effectively neglect it. However, on Vcc windings or bias windings, the diode operates close to its knee where the incremental resistance is high and you need to account for it. Otherwise, the compensation you will make is likely to be false and your design might oscillate in production. Thanks to SPICE and an accurate diode model, Rd is automatically included in the simulation. Figure 3-7e and 3-7f unveil the simulation results compared to the true measurements with a network analyzer and confirm the validity of our approach.

Switched

A simple voltage-mode FLYBACK converter is proposed by Figure 3-8a. The sketch shows the PWMVM model and a nonisolated feedback network. If needed, any kind of feedback can be implemented as previously illustrated. (Also see Figure 3-8b.)

The application makes use of a dual-output transformer in case the auxiliary winding would supply the IC's Vcc line.

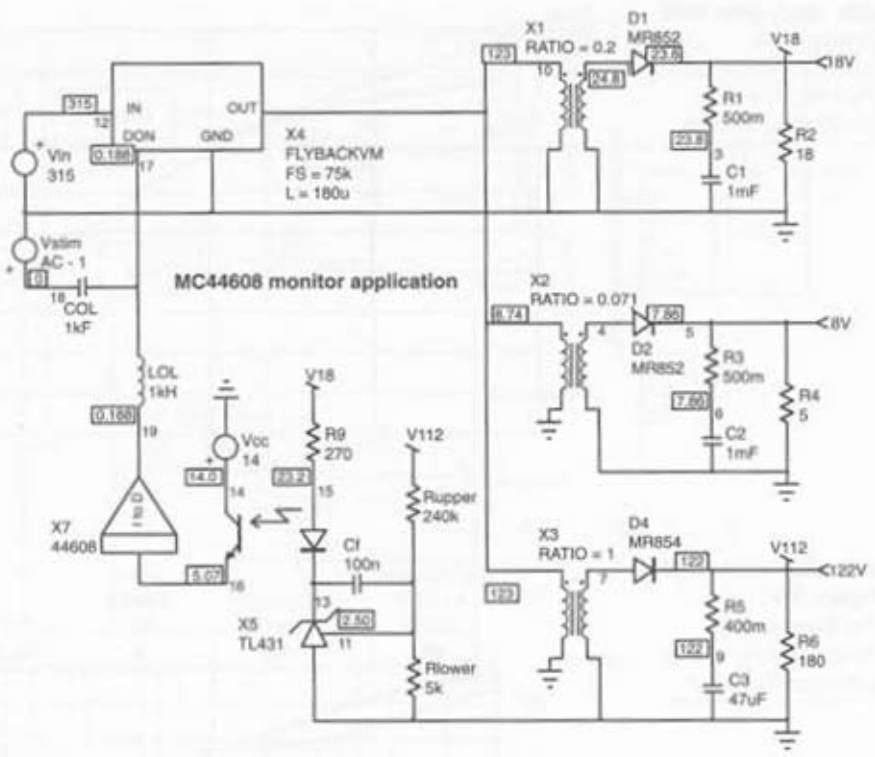


Figure 3-7d
A typical application of the MC44608 shunt regulator.

FLYBACK Current-Mode

As mentioned earlier, the current-mode version of the FLYBACK monitors the peak current circulating in the primary inductance Lp. When it reaches the final setpoint Ip, the internal latch resets and the MOSFET driving signal goes low, waiting for the next cycle. Some recent circuits monitor the true primary demagnetization and prevent the main switch to be turned-on again; you operate in free-run, also called borderline operation. This is the case of the MC33364 as we will later see.

Equations

Following are the equations for a current-mode control FLYBACK converter operating in CCM or DCM. These equations, as well as the ones later

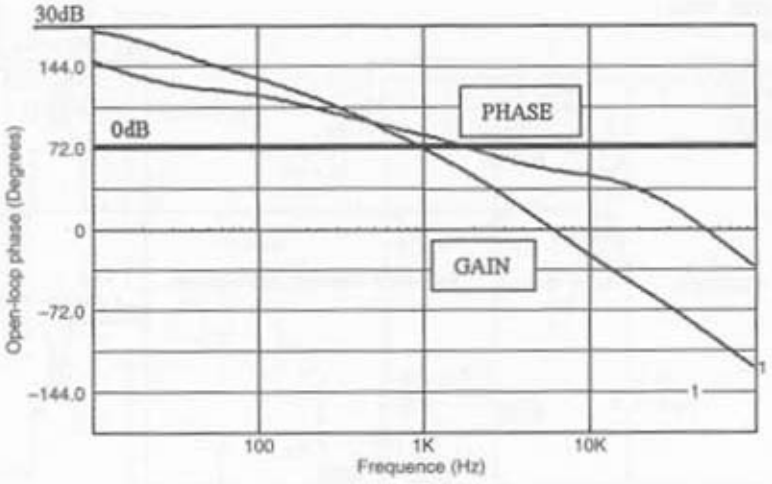


Figure 3-7e
Simulation results of the 44608 in a multioutput system.

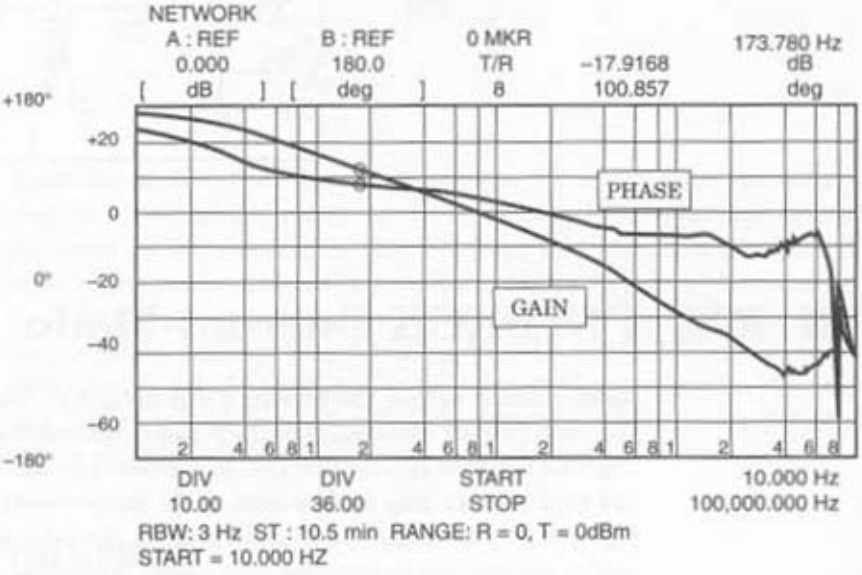


Figure 3-7f
Real bandwidth measurements of the same configuration.

given, are a compilation of results found in references [15, 19, 20, 21]. Equations do not differ much from that of the CM BUCK-BOOST except that the k ratio needs to be scaled by a ratio 1/N (primary sensing versus secondary coil expressions). (See Table 3-8.)

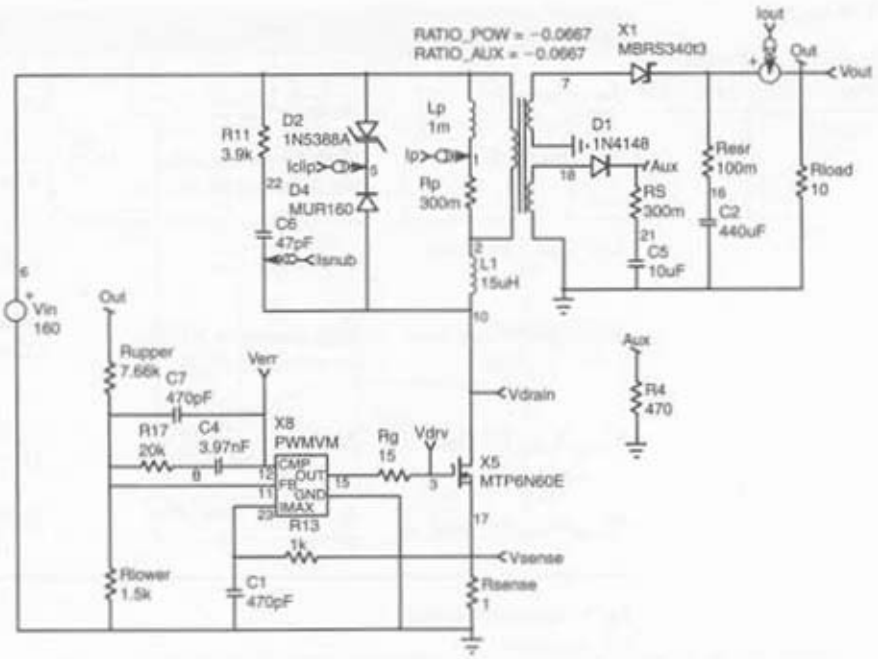


Figure 3-8a
A typical nonisolated FLYBACK converter.

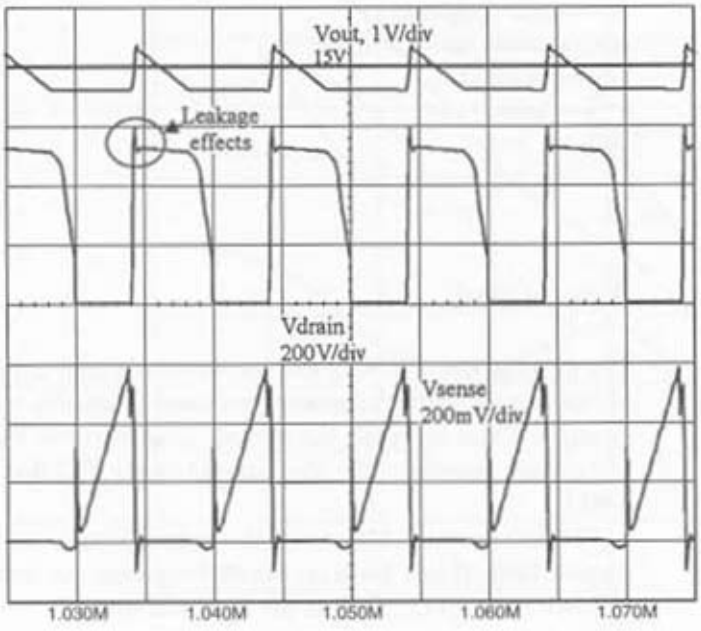


Figure 3-8b
Resulting simulation curves showing the leakage effects.

Table 3-8

FLYBACK Current-Mode Equations.

	DCM	CCM
1st-order pole	$\frac{1}{\pi \cdot R_{load} \cdot C_{out}}$	
2nd-order pole	High frequency pole, see reference [5, 21]	$\frac{(1-D)}{2 \cdot \pi \cdot \sqrt{Lsec \cdot C_{out}}}$
Left Half-Plane Zero	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [5, 21]	$\frac{R_{load} \cdot (1-D)^2}{2 \cdot \pi \cdot Lsec \cdot D}$
V_{output}/V_{input} DC Gain	$N \cdot D \cdot \sqrt{\frac{R_{load}}{2 \cdot Lsec \cdot Fsw}}$	$\frac{D}{(1-D)} \cdot N$
V_{output}/V_{error} DC Gain	$\frac{k}{N} \cdot \sqrt{\frac{R_{load} \cdot Lsec \cdot Fsw}{2}}$	$\frac{k \cdot Rload}{N} \cdot \frac{Vin}{2 \cdot Vout + Vin}$

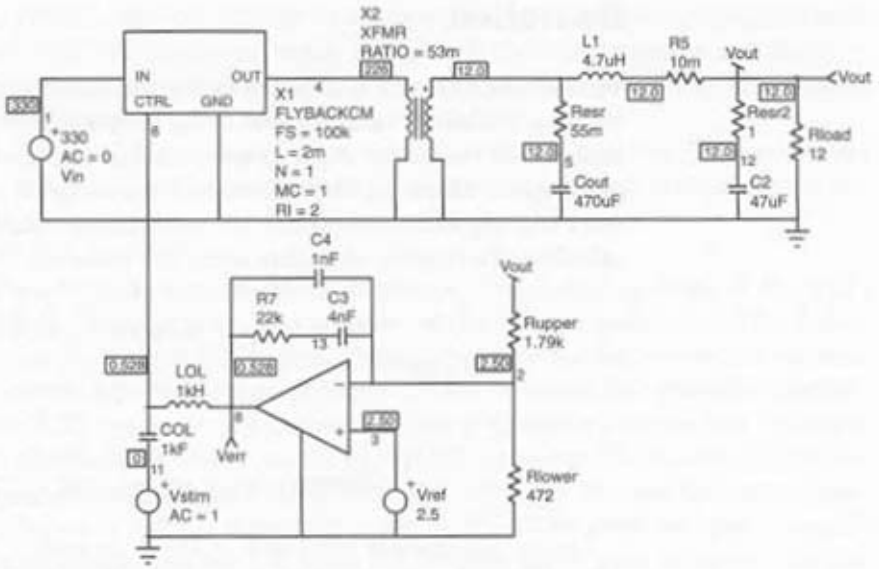
F_{sw} = switching frequency
D = duty-cycle
R_{ESR} = output capacitor's Equivalent Series Resistor
Cout = output capacitor
Vin = input voltage
Vout = output voltage
Lsec = secondary inductor = Lp · N^2
Vc = control voltage
k = max. Ipeak/max. Vc
Ipeak = k · Vc

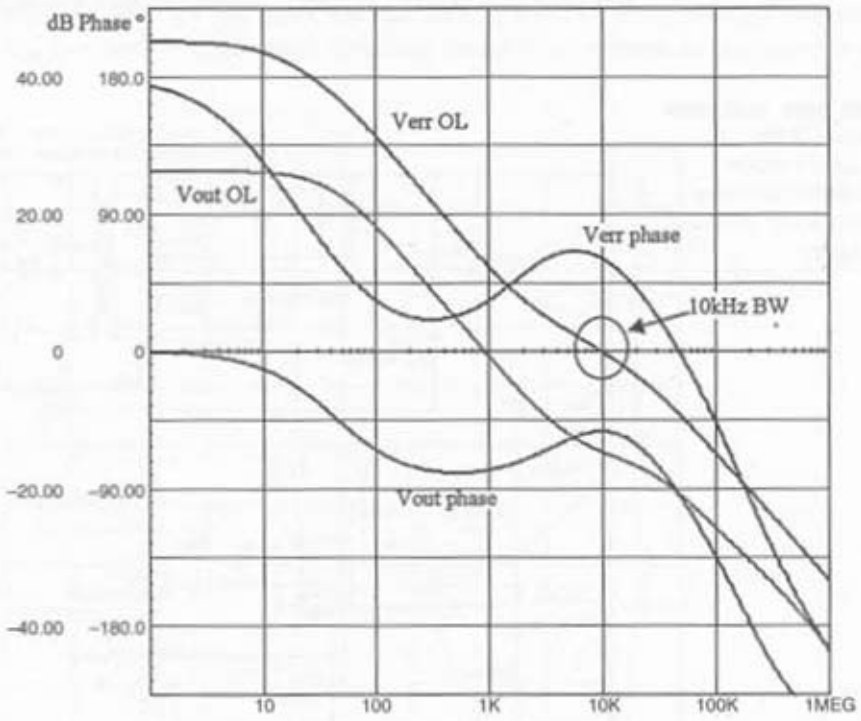
Averaged

The average simulation of the current-mode does not differ much from that of the voltage-mode. However, you need to ensure enough error amplifier swing in order to reach the correct peak current. Figure 3-8c details the simulation template for the current-mode FLYBACK. (Also see Figure 3-8d.)

The LC network filters out the output ripple mostly generated by the output ESR. If you keep its cutoff frequency far away from the targeted bandwidth, it will not affect the final stability.

Figure 3-8c, Figure 3-8d
The secondary LC filter does not jeopardize the SMPS stability.





Switched

The switched version is depicted in Figure 3-8e. The application values differ from the above example, but the principle remains the same. We have suppressed the active clipping network and replaced it with an RC type. Although it offers an immediate cost reduction, it unfortunately suffers from a strong dependency upon the maximum peak current Ip [22]. You can calculate the clipping elements using the following formula:

$$Rclamp = \frac{2 \cdot Vclamp \cdot \left(Vclamp - (Vout + Vf) \cdot \frac{1}{N} \right)}{Lleak \cdot Ip^2 \cdot Fsw}$$

$$Cclamp = \frac{Vclamp}{Vripple \cdot Fsw \cdot Rclamp}$$

Design parameters are Lleak = 15µH, Ip max = 400mA, Vout + Vf = 16V, N = 66.7m, Fsw = 100kHz, and MOSFET BV_{DSS} = 600V. The clamping level must be selected between 40 and 80 volts above the reflected output voltage when the supply is heavily loaded. The reflected output voltage

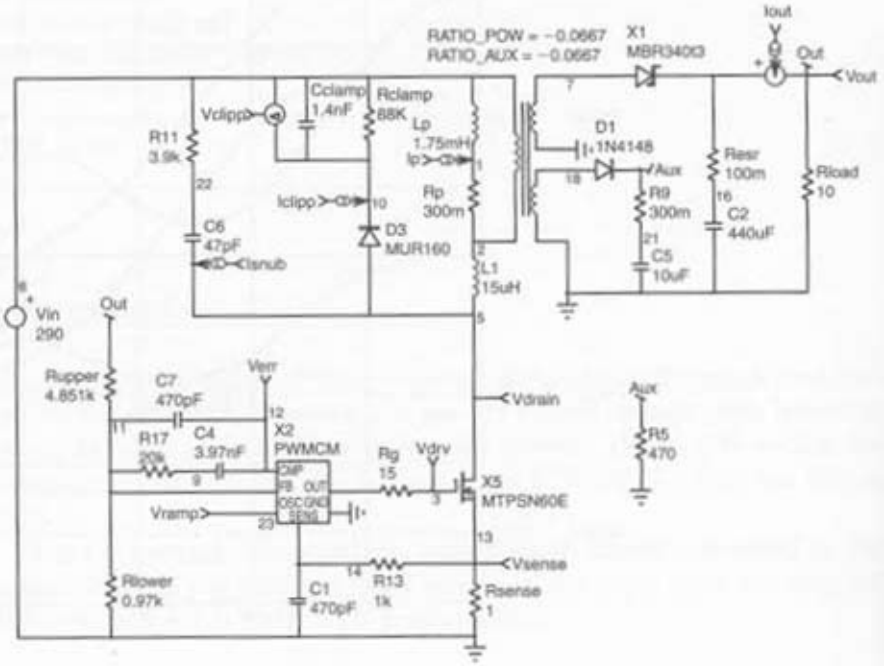


Figure 3-8e
A current-mode FLYBACK converter using an RC clipping network.

is (Vout + Vf) · 1/N = 242V to which we add 40V, implying a clamping level of 280V. The maximum drain voltage will therefore grow up to Vclamp + Vmains = 280 + 250 = 530 < BV_{DSS}. The ripple is selected at 20V. Results give Rclamp = 88kΩ and Cclamp = 1.4nF.

Figure 3-8f portrays the simulation results at high line. The drain level is safely clipped below 600V; the average clipping level corresponds to our expectations.

Two-Switch Voltage-Mode Version One major problem of the FLYBACK finds its root in the presence of the leakage inductance. This inductance strongly degrades the efficiency, but also the open-loop gain because it forces a portion of the primary current to divert into the clamping network. To overcome this problem, Figure 3-8g shows a two-switch version of a 360W offline current-mode FLYBACK converter. The model simply provides a floating output duplicating the main one. You can therefore implement a low $RDS_{(ON)}$ N-channel power MOSFET. To avoid the open-loop gain degradation, you need to reset the leakage inductance as quickly as you can. Keep in mind that any current that circulates in the leakage inductance also flows in the primary. As a result, when the above clipping network dissipates a lost heat, it steals away a portion of the primary current. The two-switch application elegantly solves this problem at the expense of

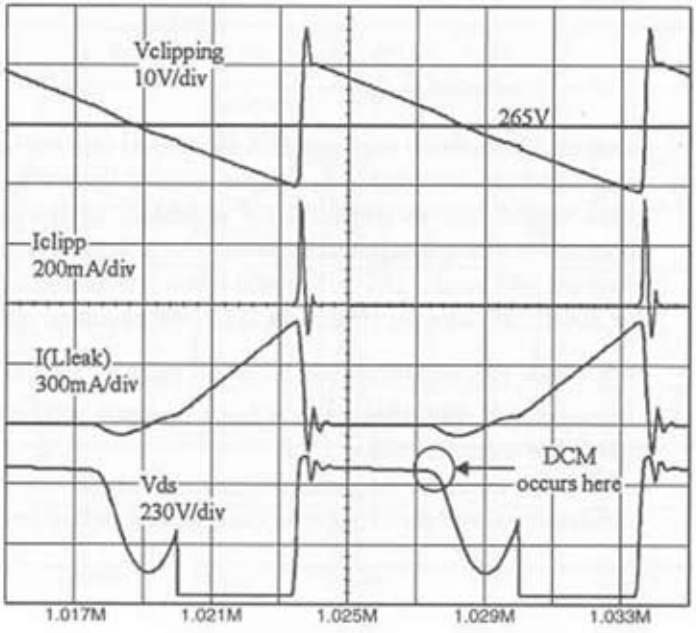


Figure 3-8f
Simulation results agree with the calculation results.

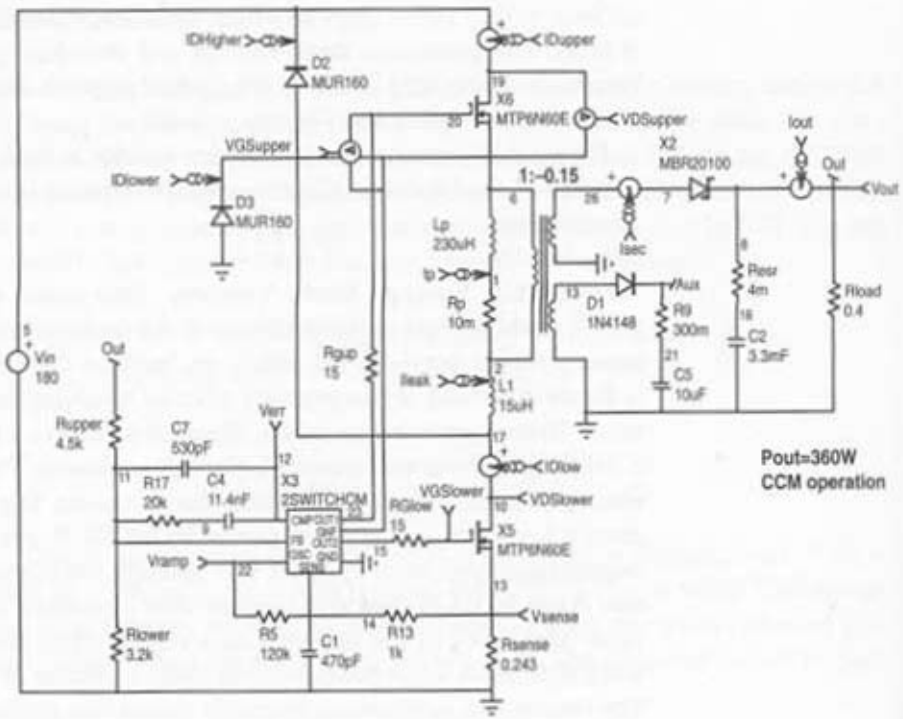


Figure 3-8g
A two-switch FLYBACK converter represents a possible alternative to the leakage inductance problem.

a second transistor and two fast diodes. At the switches' opening, the primary and the leakage inductances reverse their voltage. The primary current would like to immediately establish in the secondary but cannot because of the leakage inductance, which delays the event. The secondary current will equal (1/N . α . Ipeak) when the leakage inductance will totally be reset. The smaller this reset time, the closer to one a will be. As you can see from the schematic, this reset voltage equals $Vin - \frac{(Vout + Vf)}{N}$. Increasing N diminishes the reflected output voltage and therefore diminishes the transfer delay.

Finally, because the switches now operate in series, their BV_{DSS} can significantly be reduced to the advantage of a better (smaller) $RDS_{(ON)}$.

Our simulated waveforms appear in Figure 3-8h. It clearly reveals the time needed to reset the leakage inductance. With a 1:0.15 transformer ratio, the secondary should normally catch up at Ip/0.15 but cannot because of the leakage inductance.

FORWARD Voltage Mode

The FORWARD converter represents one possible extension of the BUCK converter, as Figure 3-9a shows.

How It Works

When the switch closes, it applies Vin . N to the secondary side through D1 and forces the inductor current to ramp up with a slope of $\frac{N \cdot Vin - Vout}{L}$.

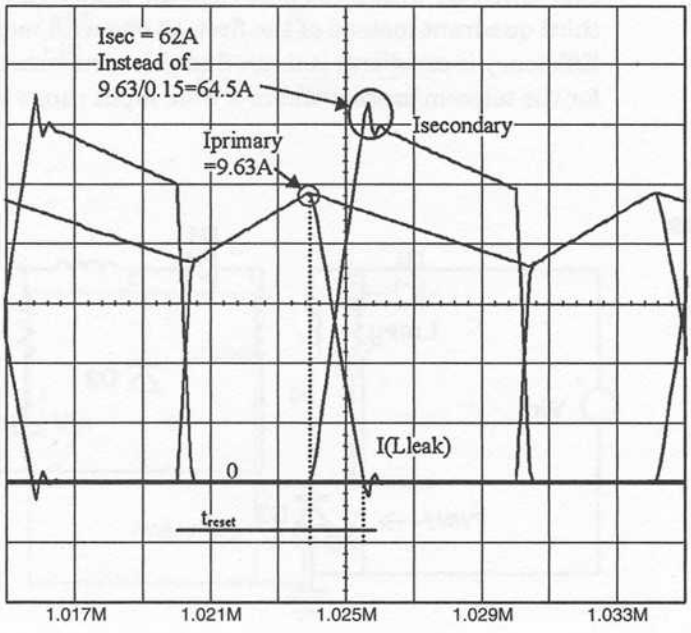


Figure 3-8h
The simulation result shows a loss of 3-8 percent of the primary current fortunately sent back to the bulk capacitor.

When the switch opens, D2 ensures the amps-turns continuity of L, exactly as in the BUCK converter case, and the inductor current ramps down with a $\frac{-Vout}{L}$ slope. However, the transformer primary magnetizing inductance needs to be reset before the next cycle begins. The reset can be implemented in several ways:

1. With an auxiliary winding as shown on Figure 3-9a—with a 1:1 ratio, the duty-cycle cannot exceed 50 percent, and the main switch undergoes 2 · Vin. When the switch opens, D3 conducts and couples the auxiliary winding to 2 · Vin, applying this level to the magnetizing inductor. The current ramps down.
2. Using a dissipative RC network, wired as the clipping network for the FLYBACK converter (RCD network)—this is a rather poor method to reset the core, but sometimes implemented when a fast diode associated with the auxiliary winding explodes the cost limit. Nevertheless, this option offers a duty-cycle range beyond the previous 50 percent limit.
3. Active clamp— this solution consists of replacing the diode in the RCD network by a controlled switch. The first purpose of this configuration is to clamp the primary to the reset capacitor, as the normal diode would do. By further controlling the time during which the switch is operated, you can implement *Zero Voltage Transition* (ZVT) on the low-side MOSFET drain. You also force the transformer to operate in the third quadrant instead of the first, as one with methods 1 and 2. Efficiency is excellent; you can find this structure in DC/DC converters for the telecom market where a wide input range is required. As with

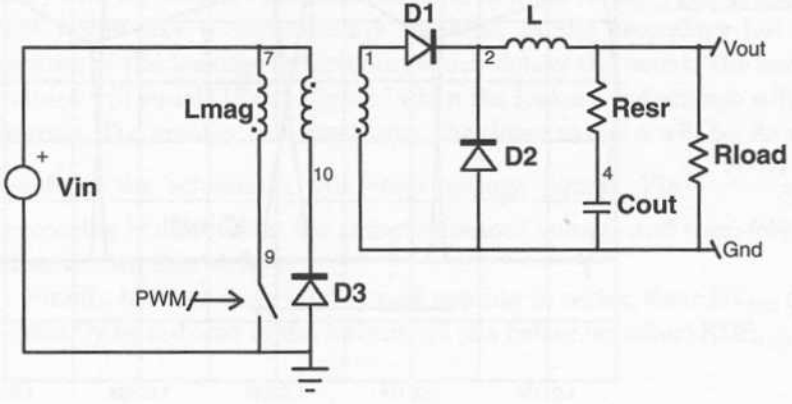


Figure 3-9a
A simplified FORWARD converter.

the RCD network, the duty-cycle can exceed the standard 50 percent limit.

4. Resonant demagnetization—this is a widely used method, especially in the DC/DC converter industry. It consists of forcing the primary inductance to resonate with another capacitor placed over the power switch. Figure 3-9b depicts this solution.

The major drawback lies in the capacitive power loss dissipated each time the switch closes.

Equations

We will purposely not rewrite the FORWARD equations because the BUCK ones still hold. The only changes are located in the following formulas:

In *CMM*,

- $\frac{Vout}{Vin} = N \cdot D$
- $\frac{Vout}{Verr} = N \cdot Vin$

In *DCM*,

- $\frac{Vout}{Vin} = N \cdot \frac{2}{1 + \sqrt{1 + \frac{8 \cdot L \cdot Fsw}{D^2 \cdot Rload}}}$

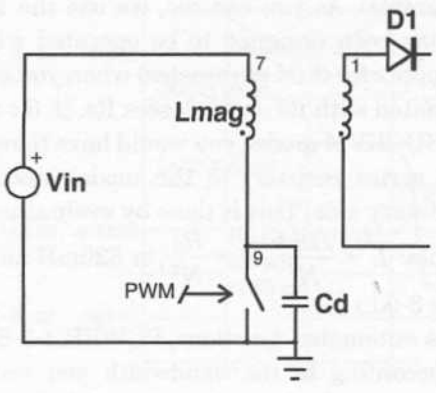


Figure 3-9b Resonant demagnetization is an elegant way of resetting the core.

- $\frac{Vout}{Verr} = \frac{\sqrt{Vin \cdot (Vin - Vout)}}{\sqrt{2 \cdot \tau_L}}$

F_{sw} = switching frequency

L = *secondary* inductance

D = duty-cycle

Rload = output load

1:N = Np:Ns transformer ratio

Averaged

FORWARD converters are usually employed in power supplies where you deliver few volts but many amps. Nevertheless, our design targets a universal offline mains converter delivering 28V@2A. The calculated components' values are the following:

Fsw:	200kHz
Lout:	130µH
Rs:	70mΩ
1:N	1:0.5
Cout:	48µF, Resr = 250mΩ
Rload:	14Ω

Figure 3-9c depicts the averaged simulation template using Ben-Yaakov's GSIM model with the PWM gain : $G_{PWM} = \frac{1}{Vsaw}$. (Vsaw = 2.5V in our example). As you can see, we use the FORWARDVM device. This element has been designed to be operated with an external transformer and accounts for it (N parameter) when you enter the output inductor value, associated with its ohmic losses Rs. If, for any reason, you would like to use the BUCKVM model, you would have to reflect the output inductance (and its series resistor) to the model since it is located on the transformer primary side. This is done by evaluating L and R through the following formula: $L = \frac{Lout}{N^2}$, $R = \frac{Rs}{N^2}$, or 520mH and 280mΩ in our example. (See Figure 3-9d.)

Thanks to its automated functions, POWER 4-5-6 tailors the compensation network according to the bandwidth you want. Later on, we will describe the k-factor method, a universal straightforward compensation tool.

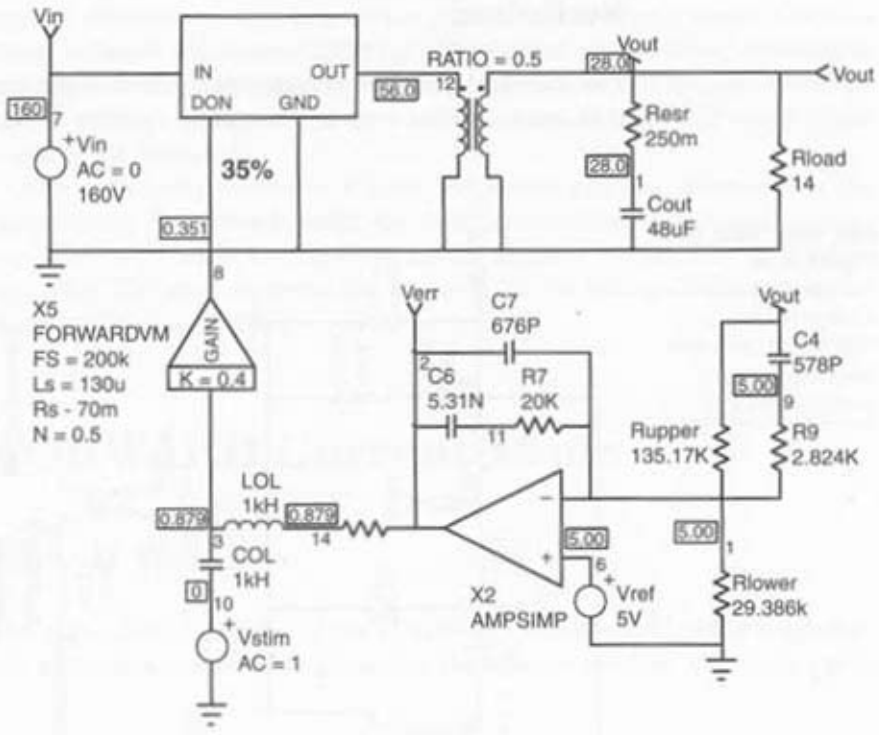


Figure 3-9c
A voltage-mode FORWARD converter delivering 28W.

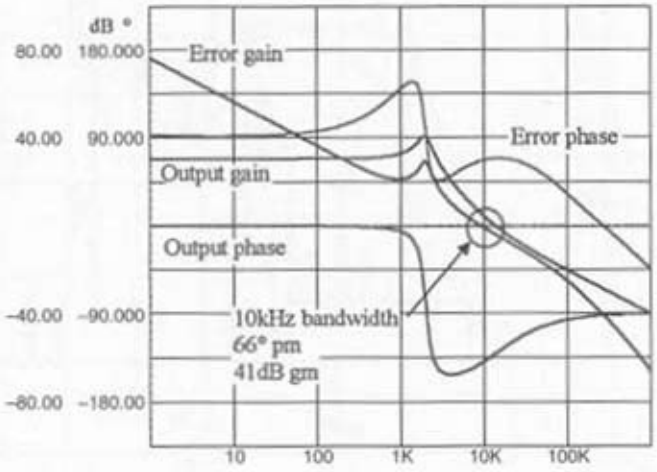


Figure 3-9d
POWER 4-5-6 compensation network offers a 10kHz theoretical bandwidth.

Switched

The switched example corresponds to the straight simulation of the Figure 3-9c example. The proposed template appears in Figure 3-9e. There is no

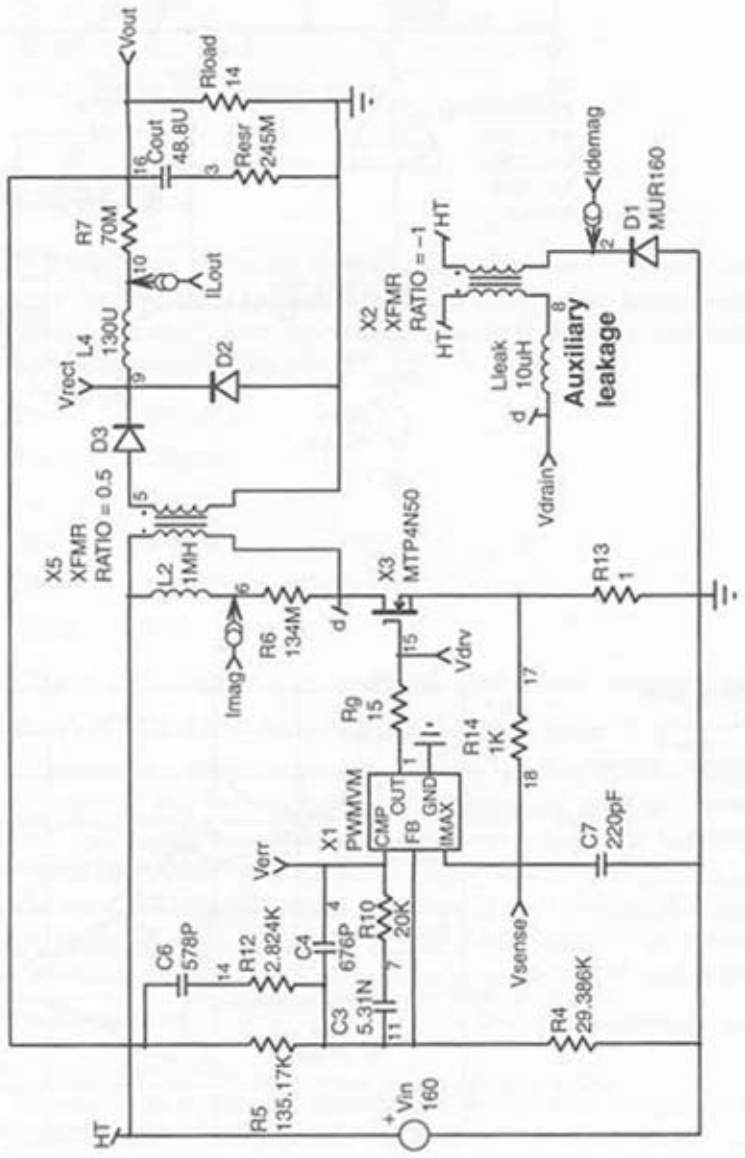


Figure 3-9e
A single switch voltage-mode FORWARD converter implementing an auxiliary winding.

specific recommendation to wire the generic voltage-mode model. The coupling between the magnetizing inductance and the auxiliary winding is ensured via another perfect transformer to which we added a small leakage inductor. You could also use several separated inductances and couple them through a k coefficient.

The waveforms appear in Figure 3-9f where you can observe how the magnetizing circulates through the auxiliary winding at the switch opening. With a 1:1 ratio, the up-slope equals the down-slope. The little spike over the VDS level confirms the presence of the leakage inductor on the demagnetization winding.

FORWARD Current Mode

How It Works

The current mode version of the FORWARD takes benefit of the magnetizing current. Thanks to its presence, there is no need to add some ramp

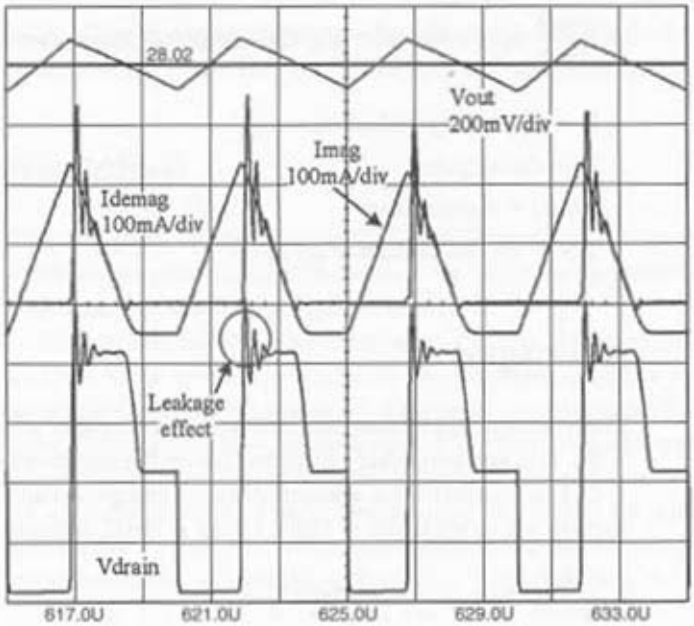


Figure 3-9f
The FORWARD requires a switch able to sustain twice the input voltage.

compensation as with precedent topologies. The magnetizing current does it naturally. The compensating ramp level is thus defined by $\frac{Vin}{Lmag} \cdot Rsense$, with Lmag the magnetizing inductance and Rsense the primary sensing network. Unfortunately, too much ramp compensation will overdamp the converter, but there is nothing you can do about it.

Equations

We will purposely not rewrite the current-mode FORWARD equations because the BUCK current-mode equations still hold. The only changes are located in the following formulas:

In *CCM*,

- $\frac{Vout}{Vin} = N \cdot D$
- $\frac{Vout}{Verr} = \frac{k \cdot Rload}{N}$

In *DCM*,

- $\frac{Vout}{Vin}$ (see reference [21] for complete description).
- $\frac{Vout}{Verr}$ (see reference [21] for complete description).

L = *secondary* inductance

D = duty-cycle

Rload = output load

1:N = Np:Ns transformer ratio

Averaged

The average simulation uses the simplest form of RIDLEY's model (Figure 3-9g). L is the secondary inductor (no reflection needed).

Let us evaluate the amount of ramp compensation that the magnetizing current offers with Vin = 160V, Lmag = 1mH, Rsense = 1Ω, and Tsw = 5µs:

- $\frac{160}{1mH} \cdot 5\mu s \cdot 1\Omega = 800\text{mV}/5\mu s$

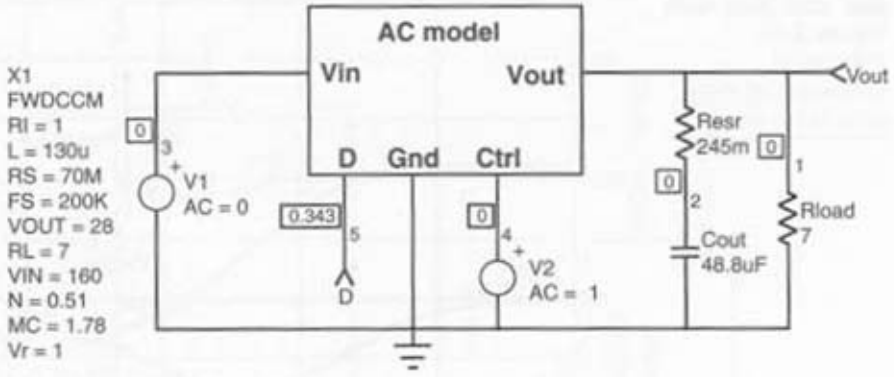


Figure 3-9g
The simplest form of Ridley's model for a FORWARD converter.

Now, let's see what is the reflected output ON slope we have over Rsense when the SMPS delivers 28V (1:N = 1:0.51):

$$\frac{(160 \cdot 0.51 - 028)}{130\mu H} \cdot 5\mu s \cdot 0.51 \cdot 1\Omega = 1.051V/5\mu s$$

If we apply Ridley's Mc definition $Mc = \frac{Se}{Sn} + 1 = 1.78$ with Se, the compensation ramp, and Sn, the secondary inductor ramp-up slope. Figure 3-9h offers the simulation results with both values of Mc: Mc = 1, no ramp compensation, and Mc = 1.78, 78 percent ramp compensation.

Switched

The complete current-mode FORWARD converter appears in Figure 3-9i. As we have stated, there is no need for ramp compensation when the internal ramp generation pin is left open.

Figure 3-9j unveils the simulation results. At start-up, the duty-cycle is pushed to its maximum value (0.45), but thanks to the natural ramp compensation, we cannot see any subharmonic oscillations. Do not think that if your duty-cycle stays lower than 50 percent you will not see any oscillations! Well below 50 percent in CCM only and without ramp compensation at all, subharmonic Fsw/2 oscillations will likely be damped and die out after a few cycles. But when you increase the duty-cycle toward the 50 percent threshold, you increase the Q and the oscillation decay takes longer to fully stop. At D = 50 percent, the Fsw/2 component is permanently in place.

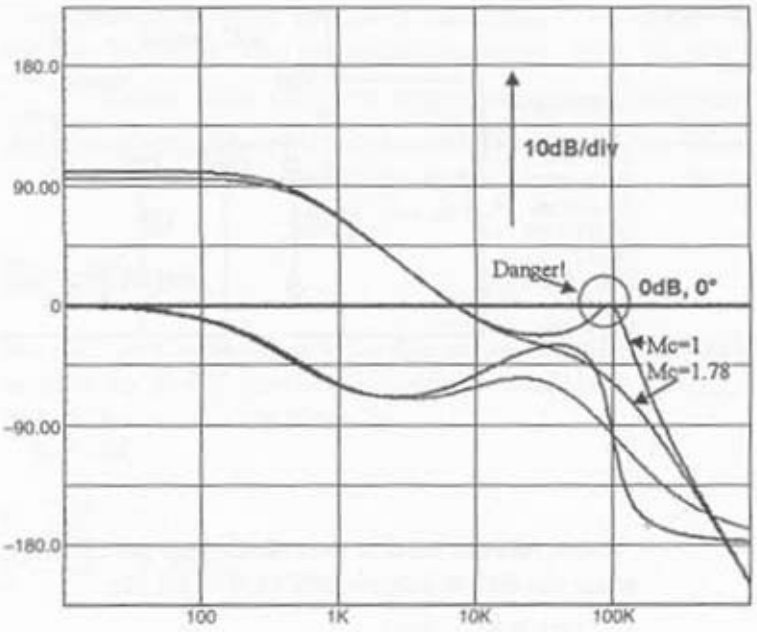


Figure 3-9h
The natural compensation ramp plays in our favor.

Thus, we strongly encourage you to inject some ramp compensation even if your duty-cycle is bounded to 45 percent, as in our example case. A good starting point is to add ramp compensation as soon as your duty-cycle exceeds 30 percent.

Forward Current-Mode, Two-Switch Version If the standard demagnetization technique requires an auxiliary winding, the two-switch version represents an elegant possible solution. The principle remains the same as for the two-switch FLYBACK converter; at the switch opening, two diodes offer a current path for the magnetizing current, which still contributes to recharge the input bulk capacitor. Figure 3-10a describes this solution.

The simulations' results detail how the leakage inductance delays the primary ramp-up at turn-on, but also delays the primary reset at turn-off (Figure 3-10b). It is a little difficult to see it on the picture, but the magnetizing current contributes to only 200mA to the free-wheel diodes' current. The leakage inductance is again the culprit for the 15-amp peak current, which forces a 2.5 Arms to flow.

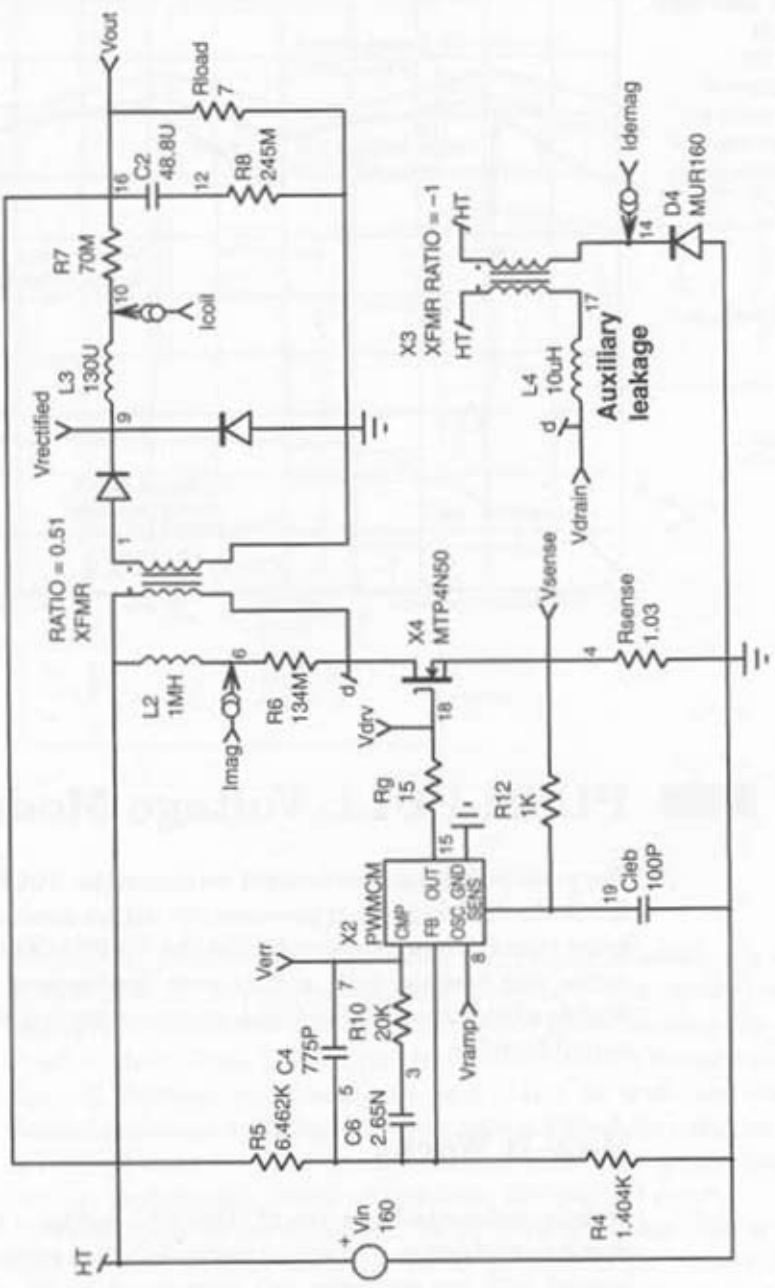


Figure 3-9i
Current-mode simplifies the compensation scheme.

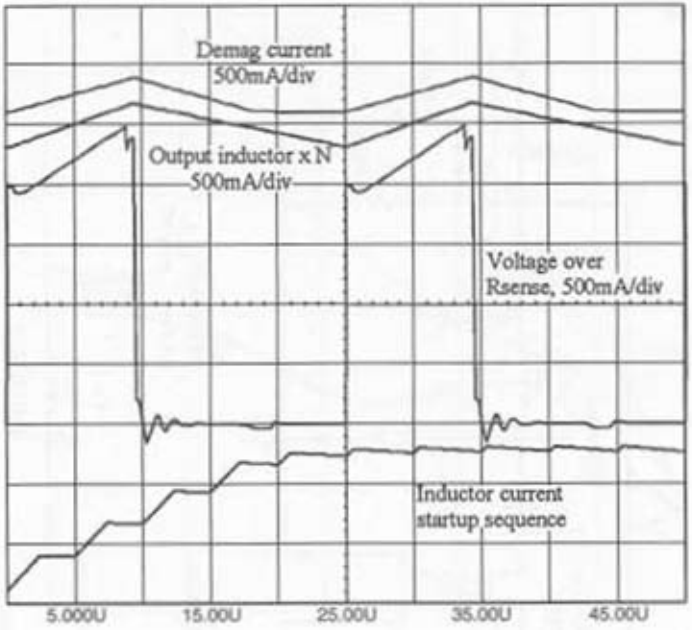


Figure 3-9j
Thanks to the demagnetization current, there is no need for an external compensation ramp.

PUSH-PULL Voltage Mode

The push-pull is another isolated version of the BUCK converter. However, thanks to the transformer presence, the output level can either be higher or lower than the input voltage. Unlike the FORWARD, the PUSH-PULL converter can operate with a duty-cycle approaching unity. Figure 3-11a depicts a traditional PUSH-PULL power-supply implementing a full bridge output rectifier.

How It Works

To fully understand how the PUSH-PULL works, it is interesting to note that its architecture actually corresponds to two single-switch FORWARDs lumped into one converter: n°1 constituted by S1, and the magnetizing inductance connected between nodes 5 and 4, while the rest of the primary (nodes 4 and 6) associated with FW2 play the role of the demagnetization

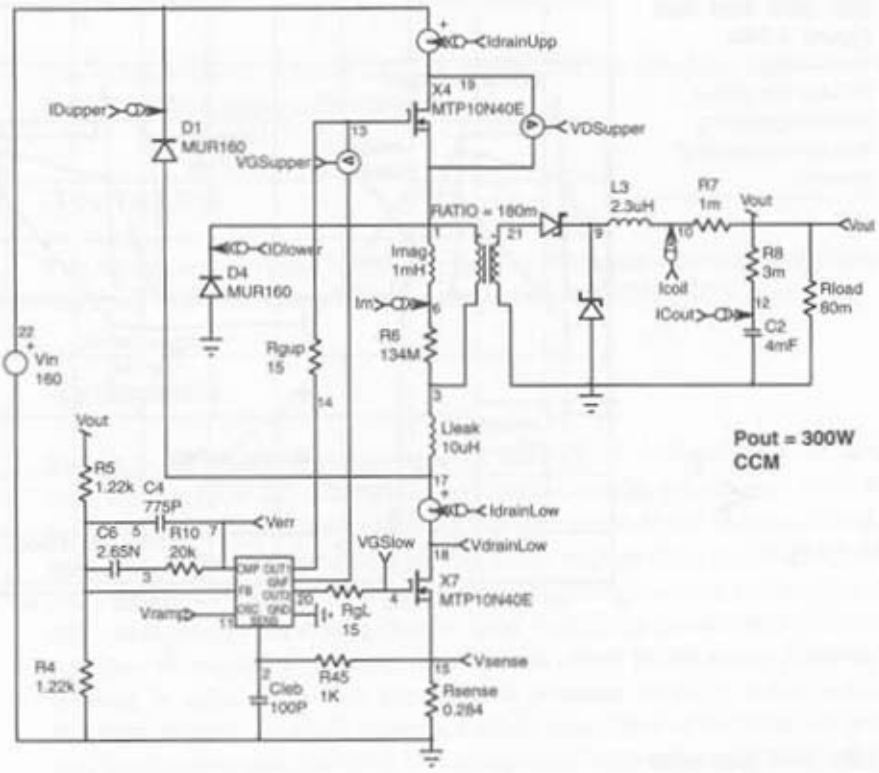


Figure 3-10a
The two-switch solution eliminates the need for an auxiliary winding.

winding. If you mirror this description with respect to node 4, you obtain the FORWARD n°2. However, be cautious; the system works exactly as two true separated FORWARDs as long as no overlap exists between the demagnetization phase of one FORWARD, and the true energy transfer of the other one [23]. Without load, this is true for $0 < D < 25$ where the magnetizing current pauses at zero for a while, just after it fully dries out. A second stage is reached when D grows up between 25 and 50 percent; the magnetizing current continuously ramps up and down without any pause.

When you load the converter, the primary free-wheel diodes no longer play any role, as the simulation will detail. You do not observe the lack of demagnetization via the primary, but rather through the secondary where the magnetization current circulates thanks to the natural coupling *between the windings.*

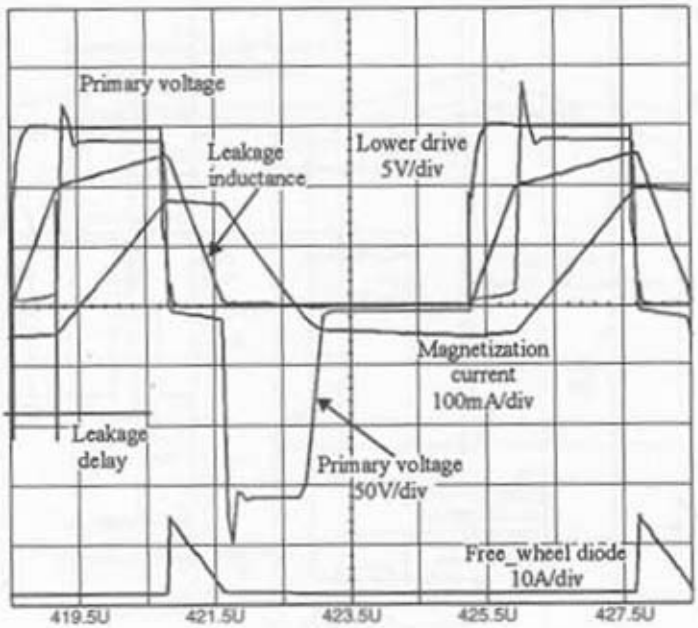


Figure 3-10b
The leakage inductance delays both magnetizing and demagnetizing instants.

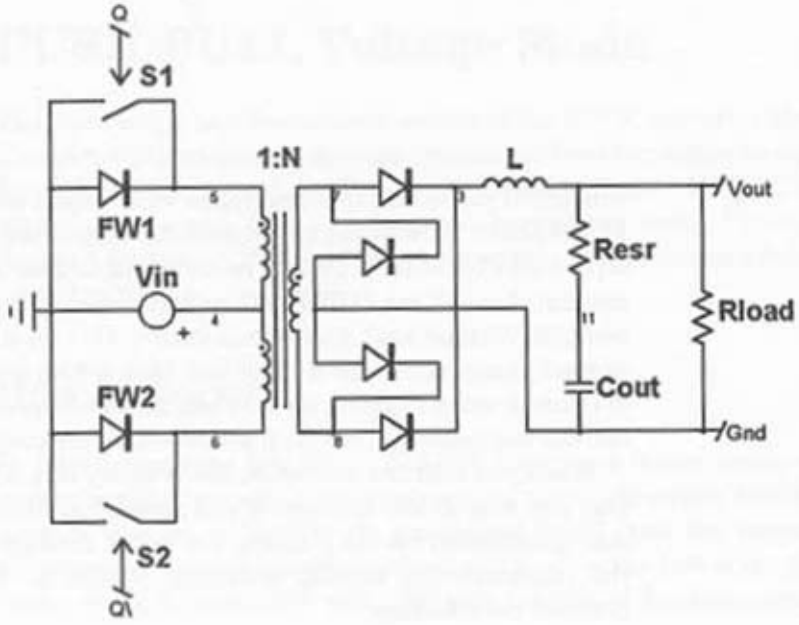


Figure 3-11a
A push-pull converter requires two extra free-wheel diodes.

Equations

The voltage-mode PUSH-PULL AC equations are identical to those of the FORWARD voltage-mode equations.

Averaged

The same remark holds for the averaged simulation where you can directly use the FORWARD simulation template for a PUSH-PULL study.

Switched

Figure 3-11b depicts a voltage-mode PUSH-PULL delivering 110W to a 7Ω load from a 160V DC source. In this first example, we equaled both transistor $RDS_{(ON)}$. Unfortunately, in a real application, there exists natural discrepancies between the switches, and their voltage drop can slightly differ. As a result, the reset voltage applied to one magnetizing inductance does not correspond to the exact opposite level that made its current ramping up; you lose the signal symmetry, and a small offset takes place. Because the current is only monitored for security reasons (a peak value within a selected acceptable level), nothing forbids this offset to continue its growth and finally saturate the core! The simulation uses our perfect transformer structure declined into a reversed center-tap version. Please note that N needs also to be reversed; RATIO = 3.91 actually means 1:255m.

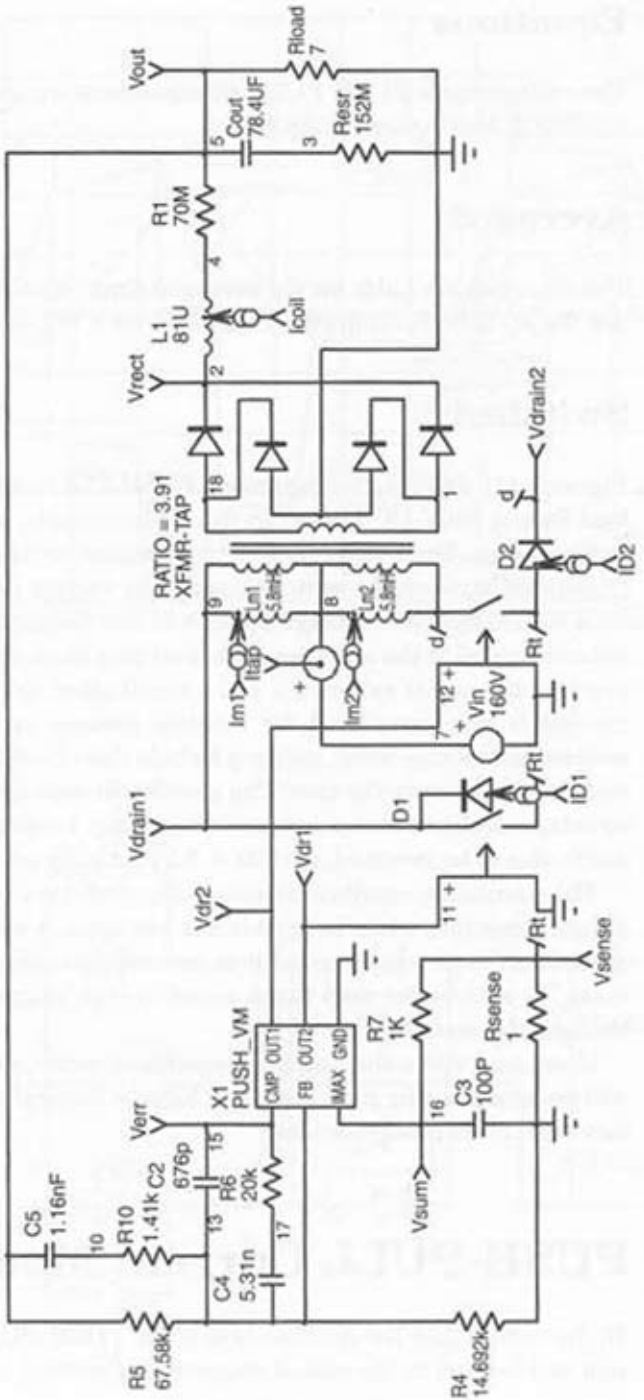
The simulation results available in Figure 3-11c confirm the pause in the magnetizing flux when both switches are open. A closer look at the diode conduction cycle would reveal it is impossible to demagnetize via the primary. To satisfy the amp-turns equation, the magnetizing current flows through the secondary.

If you now add some leakage elements in series with both switches, you will understand why good *Transient Voltage Suppressors* (TVS) are mandatory with these configurations.

PUSH-PULL Current Mode

We have seen that the Achilles heel of the PUSH-PULL voltage-mode version was located in the risk of magnetizing current runaway. The current-

Figure 3-11b
A voltage-mode PUSH-PULL converter delivering 110W.



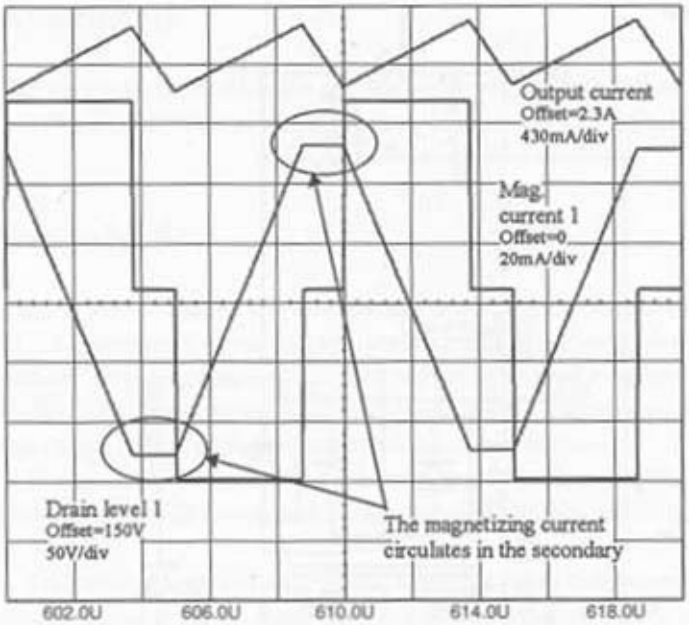


Figure 3-11c
The magnetizing current keeps flowing in the secondary when both switches are open.

mode version elegantly solves this problem by a pulse-by-pulse current monitoring.

How It Works

Thanks to current-mode control, any voltage drop unbalance will automatically be compensated by an immediate action on the opposite ON time that alternates between longer or shorter pulses. As with the FORWARD converter, an inherent ramp compensation is provided through the magnetizing current as long as the adequate level is reached.

Equations

The current-mode PUSH-PULL AC equations are identical to those of the FORWARD current-mode equations.

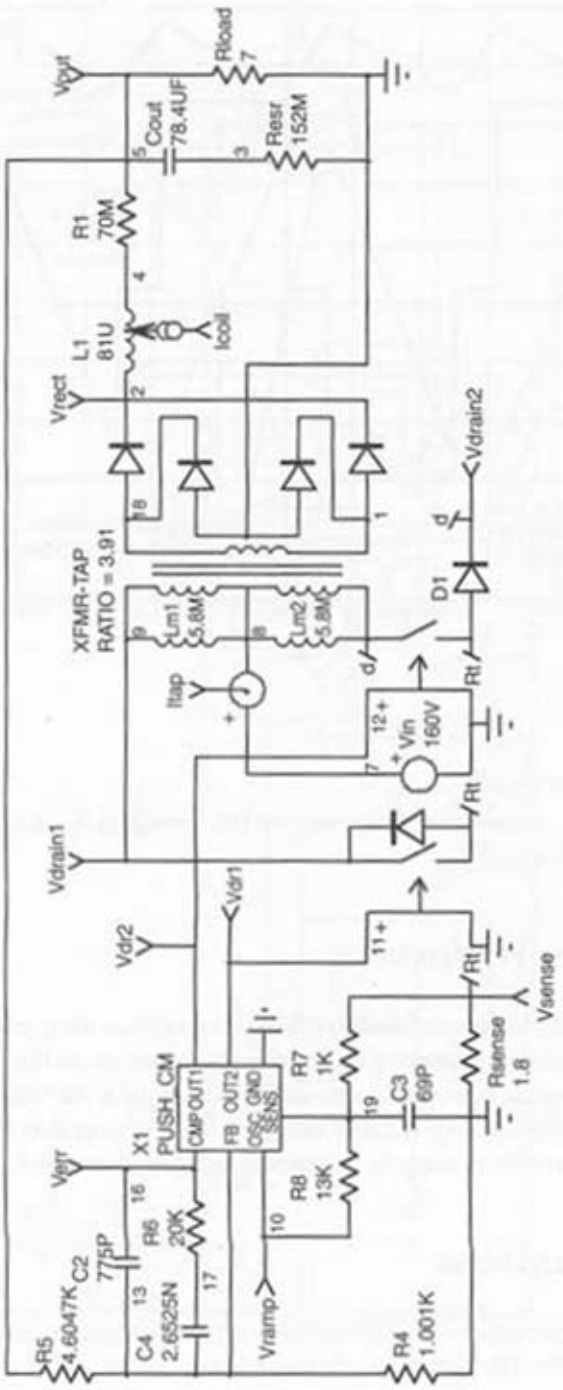


Figure 3-11d
A current-mode PUSH-PULL converter.

Averaged

The same remark holds for the averaged simulation where you can directly use the FORWARD simulation template for a PUSH-PULL study.

Switched

Figure 3-11d depicts the simulation template for the current-mode PUSH-PULL converter. As usual, the compensation network is considerably simplified. The magnetizing current behavior slightly differs from that of the FORWARD because we have two magnetizing inductors operating one after the other. How do they combine with each ON time?

Fortunately, Figure 3-11e confirms the application of the same amount of ramp at every ON time as in two separated FORWARD converters running in parallel.

However, we need to check for a correct ramp compensation through the magnetizing current. Instead of applying the standard formula "50 percent of the downslope is the ramp you need," let's apply Ridley's definitions.

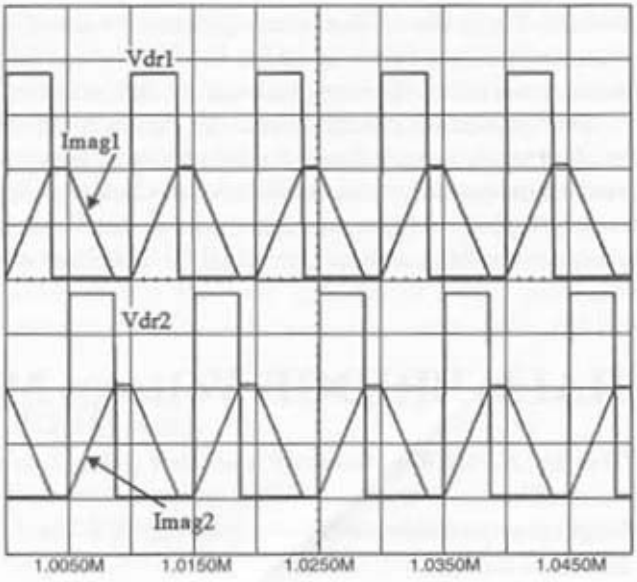


Figure 3-11e
The magnetizing current sums up with the secondary one.

The double-pole damping as defined by Ridley is identified as being the origin of Fsw/2 oscillations. We shall therefore attenuate its effects by decreasing the Q as defined by

$$|Qp| = \frac{1}{\pi \cdot (mc \cdot D' - 0.5)} = 1.67 \text{ with a duty-cycle of 69 percent or}$$

$$D' = 31 \text{ percent}$$

To properly damp the system, we need to decrease Qp to a value less or equal than 1, or $\pi \cdot (mc \cdot 0.31 - 0.5) \geq 1$. From this equation, we extract the value for mc, the compensation ramp factor: mc = 2.63 with $mc = 1 + \frac{Se}{Sn}$, Se the compensating ramp we are looking for and Sn the ON-slope of the sensed current waveform. Simply solving for Se gives the amount of compensating ramp we shall inject: $Se = 1.63 \cdot Sn = 1.63 \cdot \left[\frac{160 \cdot 0.255 - 28}{81\mu H}\right] \cdot 0.255 \cdot 1.8\Omega \cdot 5\mu s = 591$ mV/5 µs, when reflected back in voltage over Rsense.

Now, let us see what level of compensation slope the magnetizing current brings us, including a 2V saturation voltage:

$$\frac{160 - 2V}{5.8mH} \cdot 5\mu s \cdot 1.8\Omega = 145mV/5\mu s$$

To reach the above 591mV, we need to compensate for the missing 346mV. From the 5V/5µs ramp sourced by the generic model, we must attenuate it by a factor of 69.2m to obtain these 346mV. With a 1k sense resistor, we inject the ramp through a 13kΩ resistor.

The simulation results appear in Figure 3-11f where a step has been applied to the input voltage. A good transient response is typical of the current-mode operation and testifies for the lack of subharmonic oscillations.

A 50V positive input step generates a −2mV output offset. This lets you compute the DC audiosusceptibility: $20 \cdot Log(2m) = -54$dB.

HALF-BRIDGE Voltage Mode

The HALF-BRIDGE converter is another isolated version of the BUCK converter. Thanks to the dual-switch configuration, the power it can handle is larger than in single-switch versions. Figure 3-12a depicts a typical HALF-BRIDGE topology.

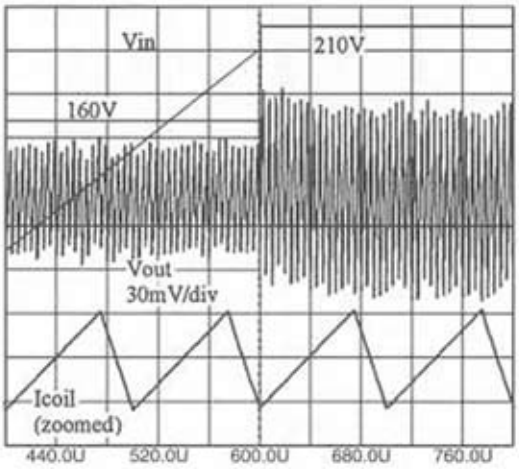


Figure 3-11f
Simulation results showing the lack of subharmonic instabilities.

How It Works

The capacitor bridge serves as a voltage divider and theoretically delivers half of the HV rail. When Q is closed, ½ HV is applied to the transformer primary and as a consequence, forces a magnetizing current into Lmag. When Q opens, Qb closes and applies the same but negative voltage to the primary, ramping down the magnetizing current in Lmag. Now you know the story; Lmag shall be fully demagnetized to avoid transformer saturation after a few switching cycles. The rectifying section remains the same as in the PUSH-PULL configuration. Since both switches SU and SL operate alternatively, the vast majority of PWM controllers incorporate a fixed amount of deadtime between the commutations to avoid any shoot-through.

Equations

The voltage-mode HALF-BRIDGE AC equations are identical to those of the FORWARD voltage-mode equations, except that we need to account for the division by 2 introduced by the capacitive bridge:

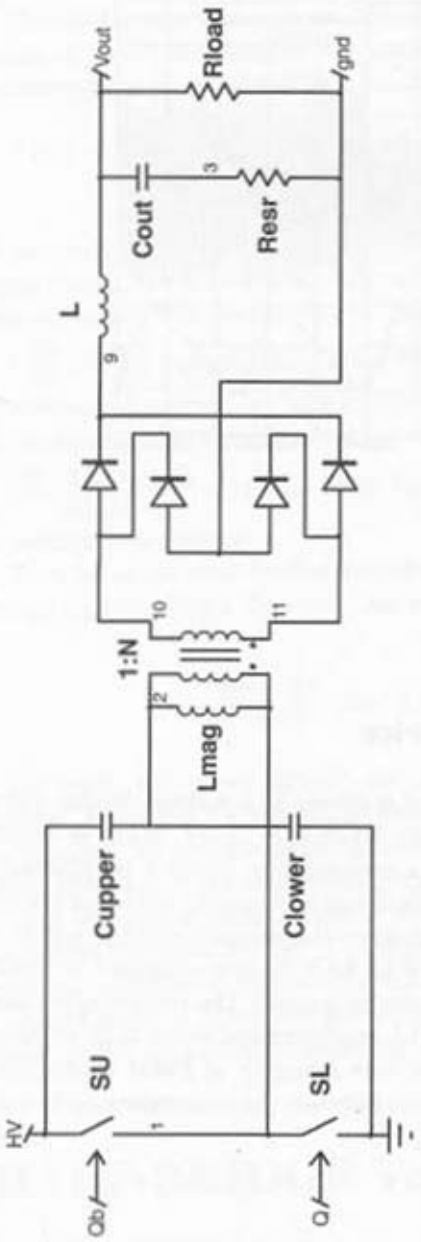


Figure 3-12a
A HALF-BRIDGE requires two specific capacitors.

In *CCM*,

- $\frac{Vout}{Vin} = \frac{N \cdot D}{2}$
- $\frac{Vout}{Verr} = N \cdot Vin$

In *DCM*,

- $\frac{Vout}{Vin} = N \cdot \frac{1}{1 + \sqrt{1 + \frac{8 \cdot L \cdot Fsw}{D^2 \cdot Rload}}}$
- $\frac{Vout}{Verr} = \frac{\sqrt{Vin \cdot (Vin - Vout)}}{\sqrt{2 \cdot \tau_L}}$

F_{sw} = switching frequency

L = *secondary* inductance

D = duty-cycle

Rload = output load

1:N = Np:Ns transformer ratio

Averaged

The same remark holds for the averaged simulation where you can directly use the FORWARD simulation template for an HALF-BRIDGE study.

Switched

We have designed a voltage-mode 110W converter operating from a 160V DC source. Because of the PWM strategy, the compensation network introduces a double zero, typical of the presence of a double pole in transfer function. Figure 3-12b portrays our simulation template. In this example, both switches are driven from a true half-bridge controller, probably using a bootstrap technique. We will see how to use a transformer if imposed by a specific controller.

Interestingly, the simulation determines the current stress values of both capacitors. The B1 source simply transforms the current flowing in R10 into voltage to implement a true pulse-by-pulse protection: *B1 19 0 V = I(R10).* Simulation results appear in Figure 3-12c.

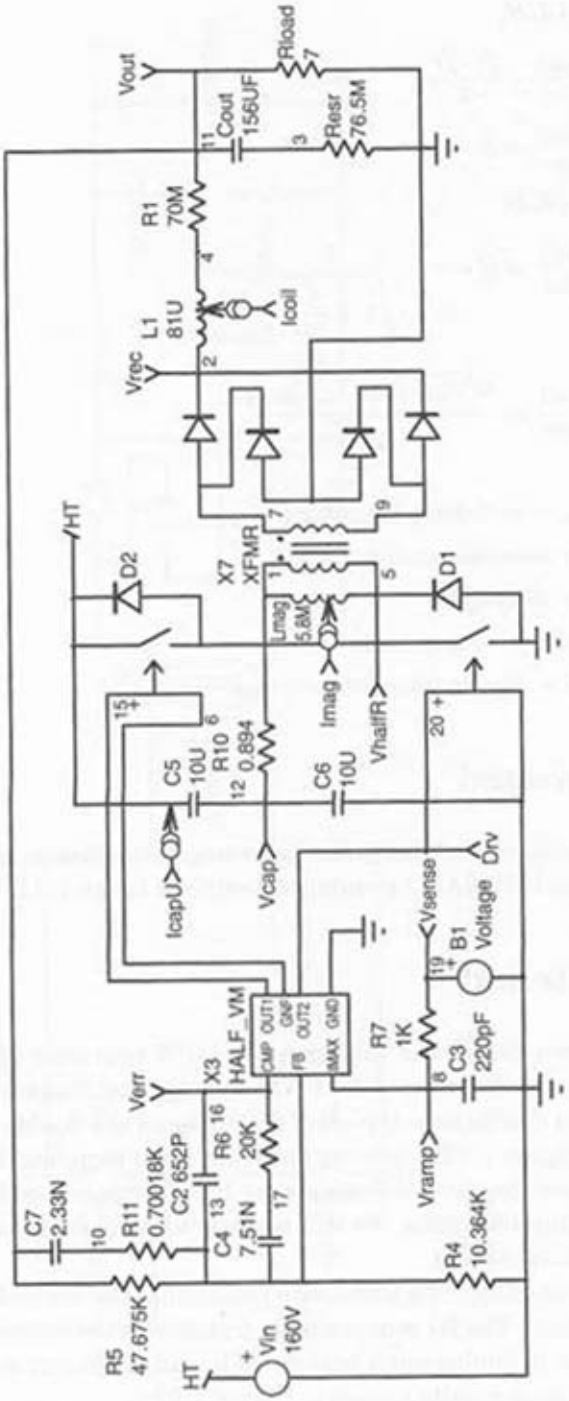


Figure 3-12b
A voltage-mode 110W offline converter.

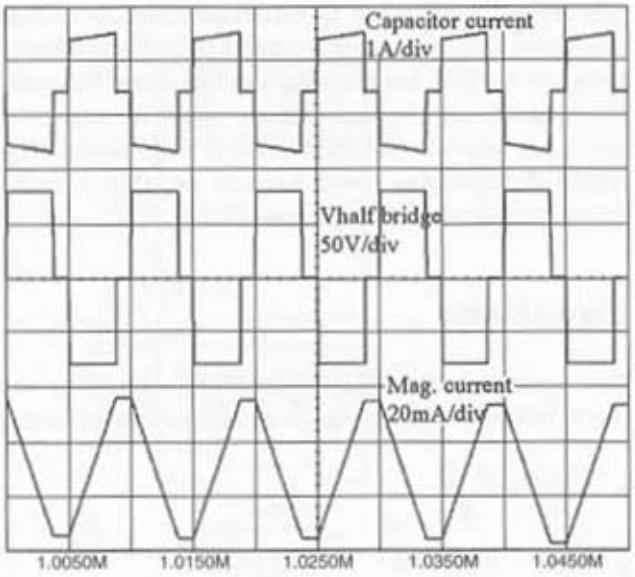


Figure 3-12c
Simulation results of the half-bridge converter.

The RMS current flowing through the capacitive bridge reaches 1A. Again, the magnetizing current exhibits a pause when both switches are open. It freewheels in the secondary, as in the PUSH-PULL case.

HALF-BRIDGE Current Mode

How It Works

The current-mode version differs from its VM counterpart by a true peak primary current monitoring. However, it can engender some capacitive voltage runaway in certain conditions. Thanks to current mode, the system naturally compensates for asymmetrical set or reset core voltages. For instance, when a switch offers a higher $RDS_{(ON)}$ than its colleague (suppose it is SL), the voltage applied to the magnetizing inductance is accordingly reduced (because of the higher drop). To fight against this result, the controller immediately lengthens the ON time to allow the proper peak current value to reach its setpoint. As a matter of fact, the charge asked to the lower

side capacitor ($Q = I \times t_{ON}$) increases and its voltage decreases. The next transition will immediately correct this effect (a lower magnetizing current slope) by further lengthening the ON time; the problem is cumulative! It finally produces a voltage runaway until the capacitive bridge gets stuck to the upper or lower rail. This is one of the reasons why current-mode HALF-BRIDGE topologies never became popular. A cure to this phenomenon exists, as described by reference [24].

Equations

The current-mode HALF-BRIDGE AC equations are identical to those of the FORWARD voltage-mode equations except that in *CCM*,

- $\frac{Vout}{Vin} = \frac{N \cdot D}{2}$
- $\frac{Vout}{Verr} = \frac{k \cdot Rload}{N}$

In *DCM*,

- $\frac{Vout}{Vin}$ (see reference [21])
- $\frac{Vout}{Verr}$ (see reference [21])

D = duty-cycle

Rload = output load

1:N = Np:Ns transformer ratio

Averaged

The same remark holds for the averaged simulation where you can directly use the FORWARD simulation template for an HALF-BRIDGE study.

Switched

Figure 3-12d offers the simulation template for the current-mode control HALF-BRIDGE converter. For the sake of understanding the phenomenon,

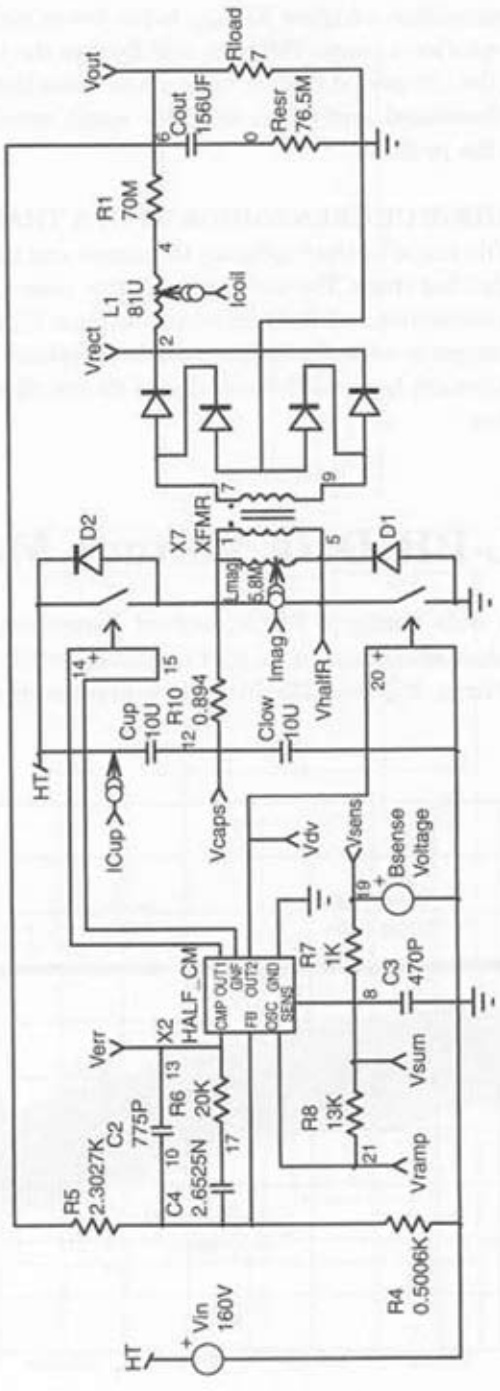


Figure 3-12d
Current-mode version of the HALF-BRIDGE converter.

we purposely assign a higher $RDS_{(ON)}$ to the lower switch. As predicted, the controller asks for a longer ON time and flushes the lower capacitor. In the next cycle, the ON period further expands because the magnetizing current slope has decreased and so on until we reach zero. Figure 3-12e clearly illustrates the problem.

HALF-BRIDGE CURRENT-MODE WITH A TRANSFORMER Some controllers do not offer the bootstrap technique and thus cannot implement a floating driving stage. The standard solution uses a transformer still driven by the controller, but floating on its outputs. Figure 3-12f depicts how to wire it properly with the current-mode template. We will not give any simulation results because the waveforms do not differ much from the previous studies.

FULL-BRIDGE Voltage Mode

Within the wide family of BUCK-derived converters, the FULL-BRIDGE topology takes advantage of its four operated switches to deliver a larger amount of power. Figure 3-13a shows how to properly wire them. Thanks to

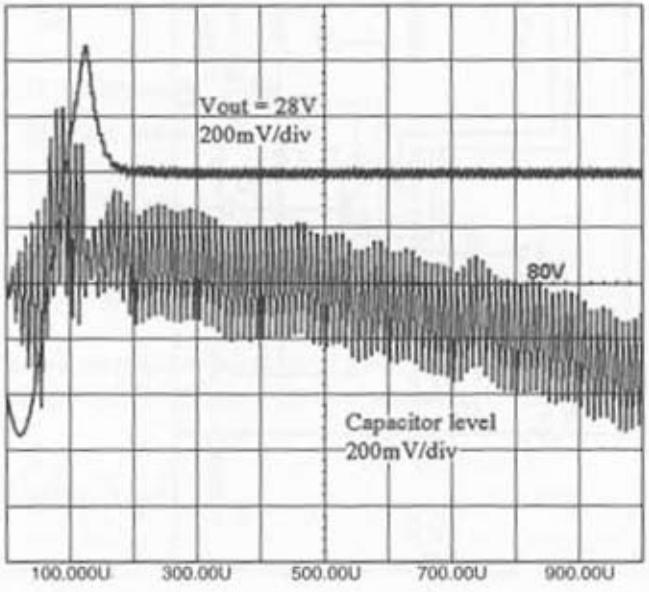


Figure 3-12e
When a switch drops more voltage than the other, you observe capacitive voltage runaway.

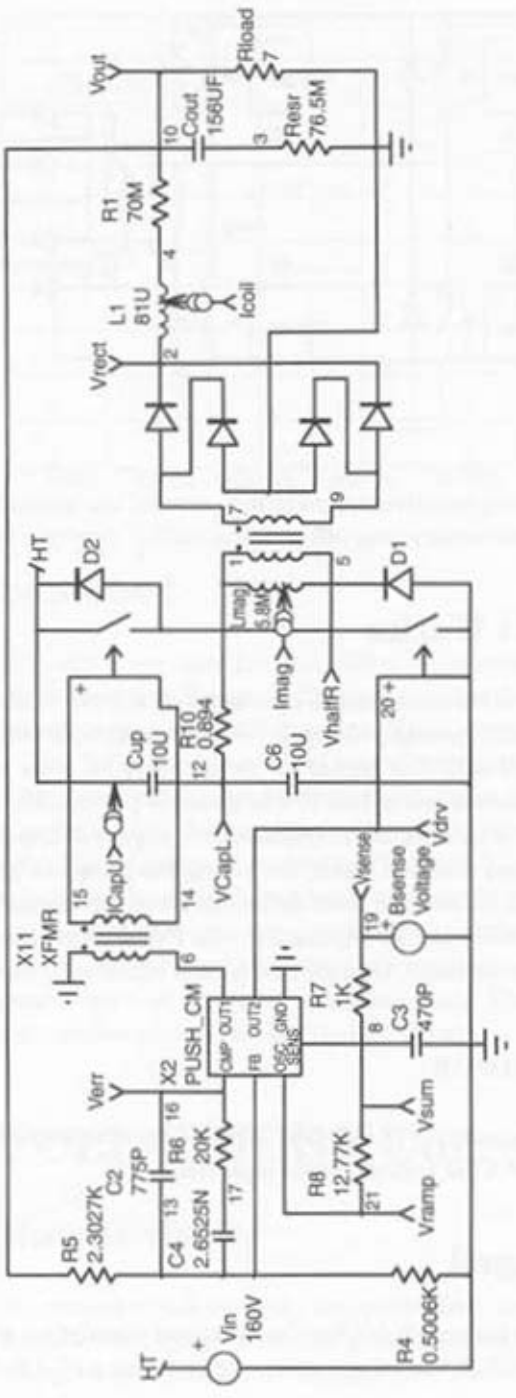


Figure 3-12f
A simple transformer overcomes the lack of floating output stage.

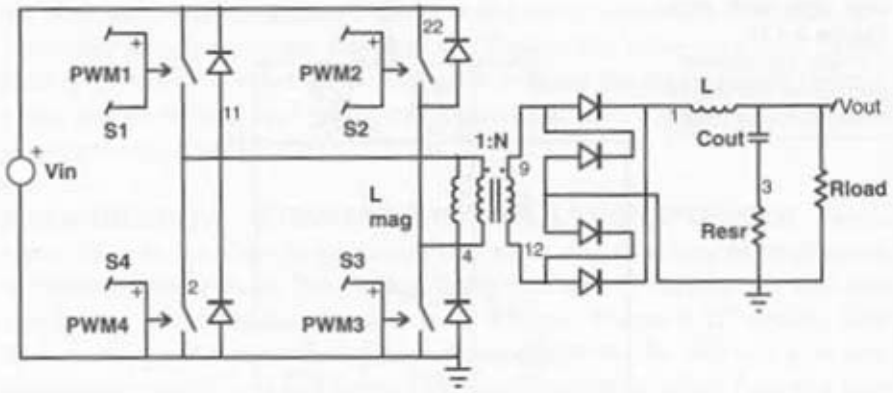


Figure 3-13a
A FULL-BRIDGE structure gangs four switches.

positive and negative magnetizing current, the transformer core operates in a very satisfactory way, offering the ability to sweep the complete B-H loop.

How It Works

Different strategies exist to alternatively operate the switches. The first one consists of separately driving two legs as S1-S4 and S2-S3 in phase. The driver will shift the signal so as to create an area where one leg is high while the other one is low. The longer this period, the larger the current will be that you force into the transformer. Figure 3-13b depicts the signals.

The other solution lies in activating the switches by opposite couples like S2-S4 and S1-S3. You thus define classical ON times for both couples. This ON time will then be adjusted by the PWM controller according to the output power demand. Our generic model adheres to this latest strategy.

Equations

The voltage-mode FULL-BRIDGE AC equations are identical to those of the FORWARD voltage-mode equations.

Averaged

The same remark holds for the averaged simulation where you can directly use the FORWARD simulation template for a FULL-BRIDGE study.

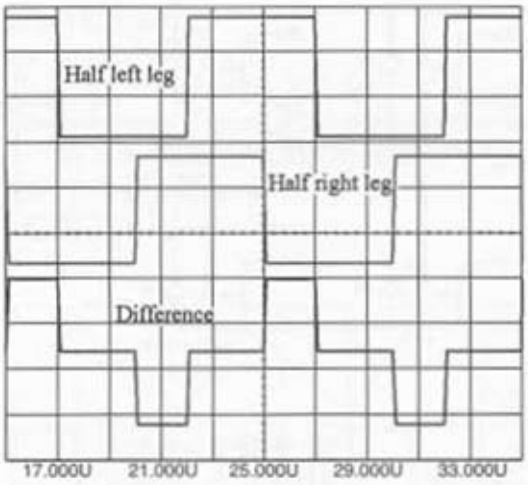


Figure 3-13b
The phase shifting method works well for full-bridge applications.

Switched

The converter example still delivers the same amount of power as the previous versions. Figure 3-13c portrays the final application schematic that increases in complexity because of the numerous switches.

The B1 source routes and transforms the primary current into a ground-referenced voltage-source needed for pulse-by-pulse current limitation. The simulation results appear in Figure 3-13d, clearly revealing the adopted modulating strategy. As for the PUSH-PULL, the magnetizing current freewheels in the secondary when both switches are open. Therefore, when one pair of switches opens, the transformer ends are floating until the next pair are closing. The magnetizing inductance combines with all the parasitic capacitors and an oscillation takes place. This explains the strange voltage curvatures on both bridge middle-points.

FULL-BRIDGE Current-Mode

How It Works

In current-mode version, the controller senses the current in a floating manner through a dedicated sense element. As usual, some ramp compensation needs to be added to fight the Fsw/2 subharmonic poles.

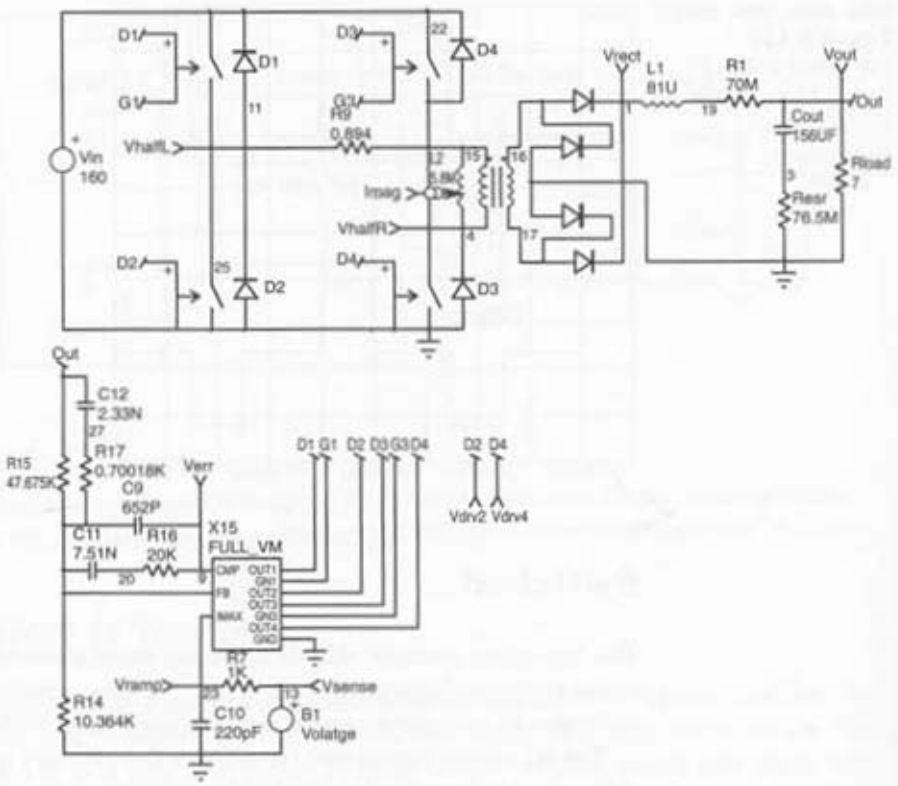


Figure 3-13c
A FULL-BRIDGE version drives up to four switches.

Equations

The voltage-mode FULL-BRIDGE AC equations are identical to those of the FORWARD voltage-mode equations.

Averaged

The same remark holds for the averaged simulation where you can directly use the FORWARD simulation template for a FULL-BRIDGE study.

Switched

The converter example still delivers the same amount of power as the previous versions. Figure 3-13e portrays the final application schematic.

The simulation results appear in Figure 3-13f detailing the startup response of the converter.

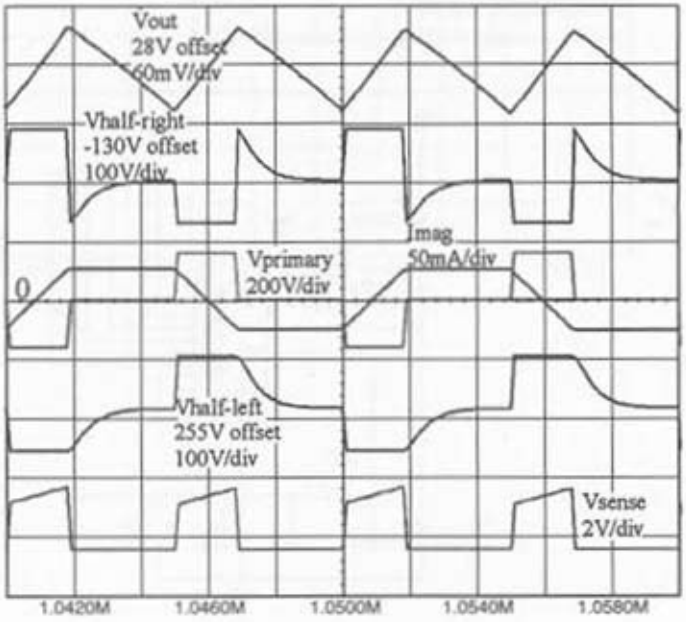


Figure 3-13d
FULL-BRIDGE simulation results.

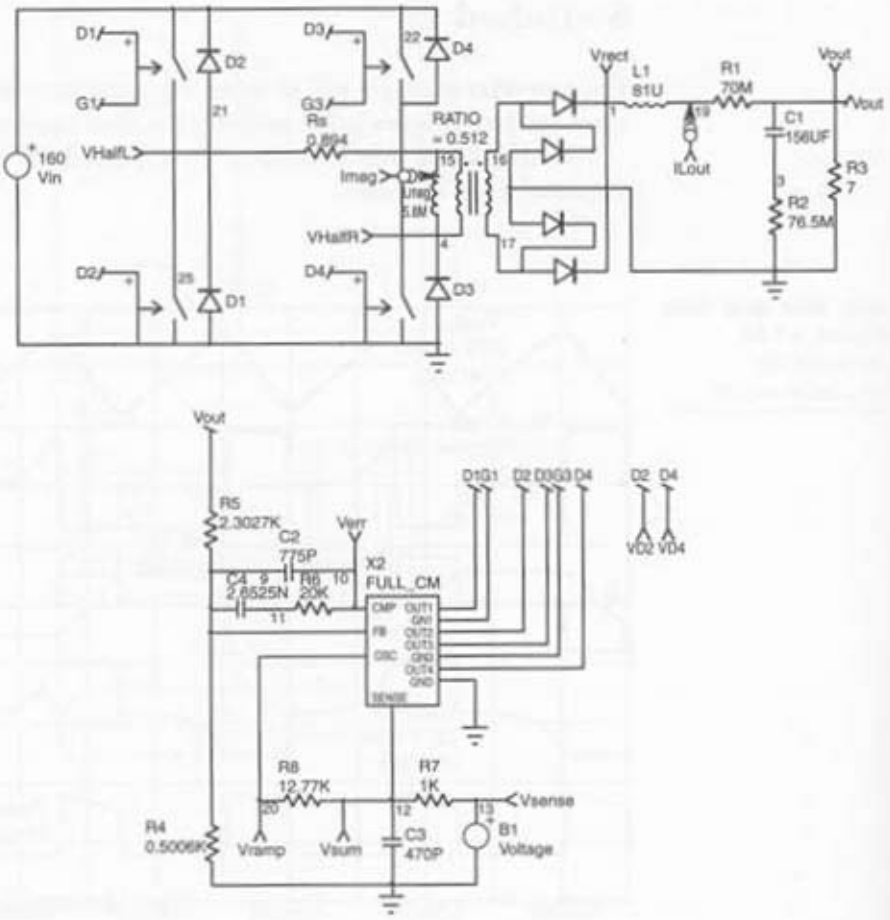


Figure 3-13e
A FULL-BRIDGE in current-mode senses the current through the transformer primary.

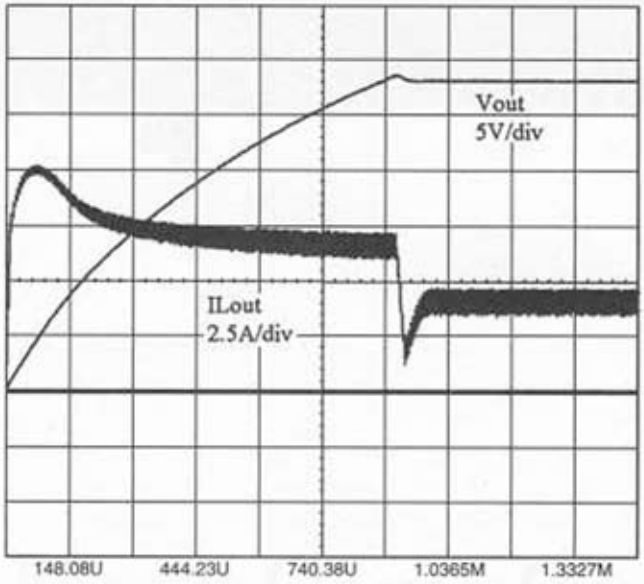


Figure 3-13f
Typical startup sequence of the FULL-BRIDGE current-mode converter.

CHAPTER 4

More Complex Simulations

In this chapter, we have gathered some converters built around less usual configurations like the SEPIC, or simply commercial ICs whose SPICE model is also available from ON Semiconductor. The description will not follow the previous structure in order to enable a faster browsing of these specific structures.

The SEPIC

The *Single-Ended Primary Inductance Converter* (SEPIC) can be thought of as the association of BOOST and a BUCK-BOOST (or FLYBACK) converter. Figure 4-1 describes a typical SEPIC architecture using coupled inductances, while Figure 4-2 represents the same converter but redrawn to allow a better understanding of the topology. The topology could also be used with two separated uncoupled inductors.

The coupling capacitor Cs plays a significant role because its offset authorizes the BOOST inductor to deal with output voltages lower than the input level. On average, Figure 4-1 shows that the right C's end (or node 1) is zero. Thus, C's steady-state voltage must equal Vin since V(Ls) is also zero on average. By applying the traditional volt-second balance to the Lp inductor, we see that during the ON time, Vin appears across its ends (because both coils are coupled) while during the OFF time, Vout is present thanks to the diode. Therefore:

$$Vin \cdot D = Vout \cdot D' \rightarrow \frac{Vout}{Vin} = \frac{D}{1-D} \text{ in CCM voltage-mode.}$$

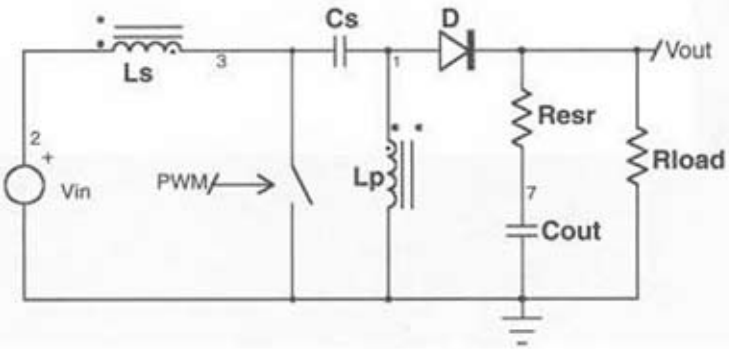


Figure 4-1
A SEPIC coupled inductance converter.

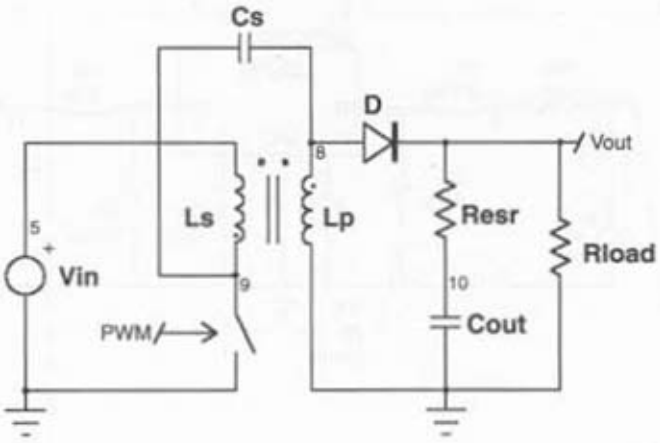


Figure 4-2
The same version highlighting the FLYBACK.

In DCM, this equation transforms in

$$\frac{Vout}{Vin} = \sqrt{\frac{Rload}{Re}} \text{ with } Re = \frac{2 \cdot [Ls//Lp]}{D^2 \cdot Tsw} \quad [21]$$

Average, Voltage-Mode

The GSIM approach greatly lends itself to the implementation of an average SEPIC simulation. For the sake of simplicity, we will adhere to the standard uncoupled version. The interested reader will find all the necessary recommendations to build such a model in reference [25]. Please note that the simulations below were carried using PSpice only. The conversion process failed to implement this model under IsSpice.

Figure 4-3 portrays our application schematic where additional input/output RFI filters have been added. The sweep source Vstim injects the AC modulation but also the necessary offset. The present simulation delivers 52V@10A.

Averaged simulation results are delivered by Figure 4-4a. You can appreciate how the numerous pole/zeroes combinations shape the final control to output curve. By stepping the input source (V1), the model is also able to predict the transient open-loop audio susceptibility (Figure 4-4b).

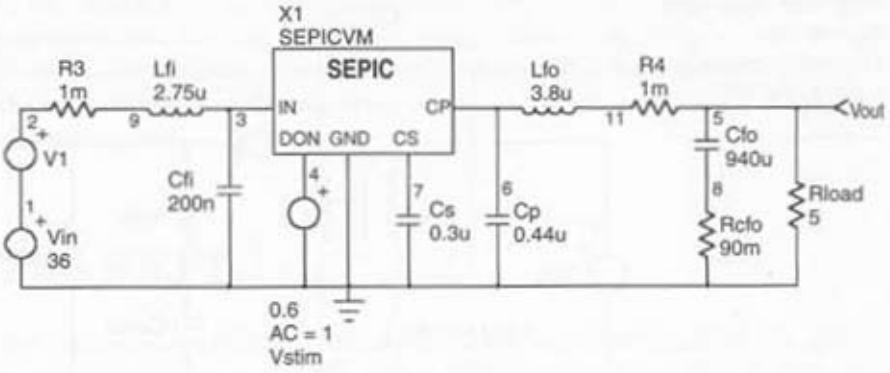


Figure 4-3
An uncoupled core SEPIC averaged simulation with external LC filtering.

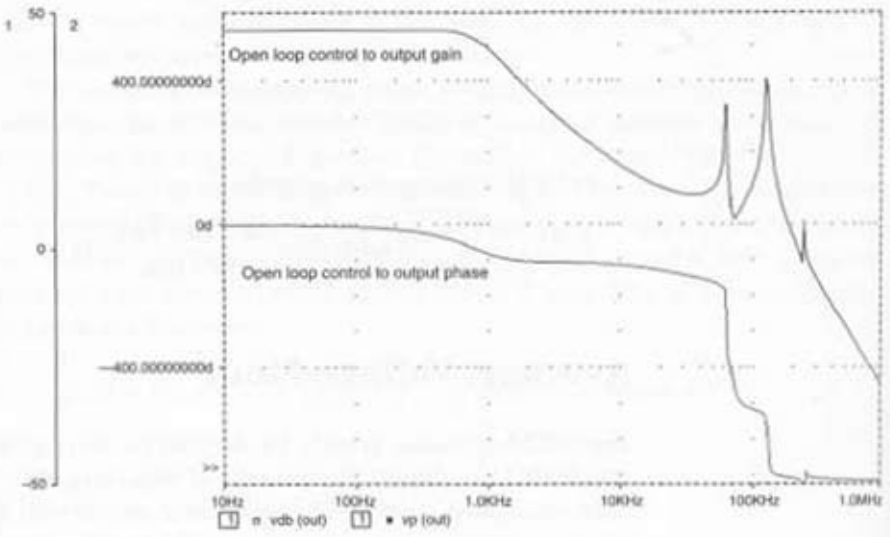


Figure 4-4a
Open-loop Bode plot of the SEPIC converter.

Average, Current-Mode

Thanks to GSIM versatility, the current-mode version simply requires the addition of a dedicated line, which combines the frequency, control voltage, and the sense resistor. This is needed to derivate the corresponding ON time. However, if you look at Figure 4-1, the current circulating through the

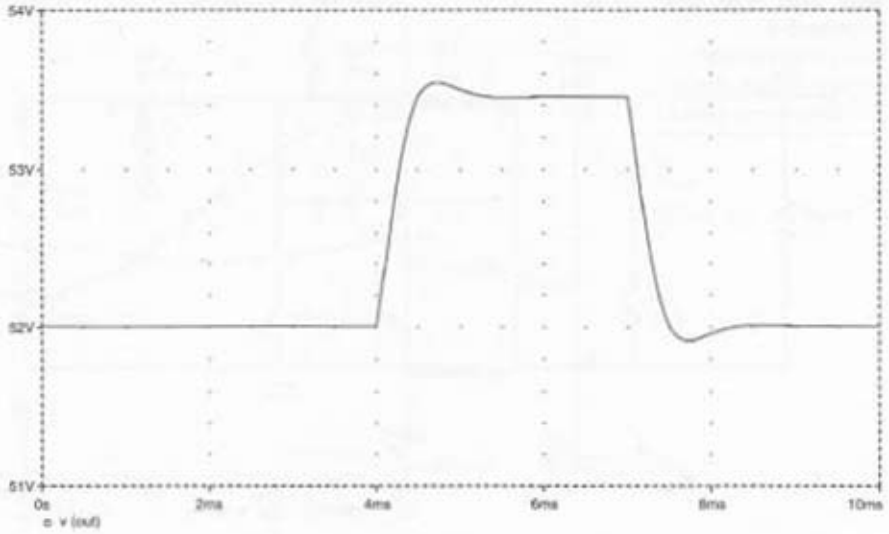


Figure 4-4b
Open-loop response to a 1V input step.

closed switch is the combination of the current through Ls (forced by Vin) but also through Lp (forced by V_{CS}). The D_{ON} generator thus looks like

$$D_{ON} = \frac{Vctrl - ks \cdot (ILs + ILp)}{Tsw \cdot \left[Mc + \frac{ks}{2} \cdot \left(\frac{Vin}{Ls} + \frac{VCs}{Lp} \right) \right]}$$

neglecting the switch ON losses with the following:

Vctrl: control voltage fed to the model

Vin: input voltage

Tsw: switching period

Mc: slope compensation in V/s

ks: sensed current conversion ratio (V/A)

Figure 4-5 plots the same operating conditions above where the voltage-mode model has been replaced by the current-mode version.

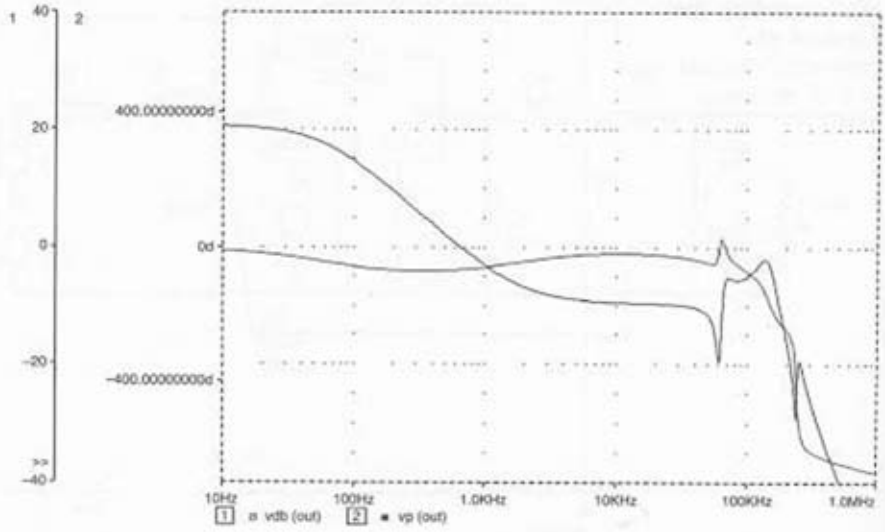


Figure 4-5
The current-mode version greatly eases the resonating peaks.

Switched

We have selected an application example using the CS322, a variable frequency controller available from INTUSOFT only. However, we also built a coupled inductor version around our generic fixed frequency model. Figure 4-6a illustrates the first application schematic made with the voltage-mode controller from Cherry Semiconductor [27]:

In this schematic, unwanted resonances have been damped with the series RC network Cs1/R1. Figure 4-6b unveils the simulation results: the series capacitor Cs undergoes an RMS current of 510mA while the output capacitor is the seat of a 2.55A RMS current.

Generic Current-Mode Sepic This simulation template appears in Figure 4-7a. The inductors are coupled via the coupling element k, which can easily emulate a leakage inductance between both windings. A large leakage inductance-Cs product contributes to lowering the input ripple current in Ls. However, at low-input voltage and high-output current (worse case), a near rectangular current flows in Cs: Iout during the ON time and I_{IN} during the OFF time. This is confirmed by Figure 4-7b simulation results.

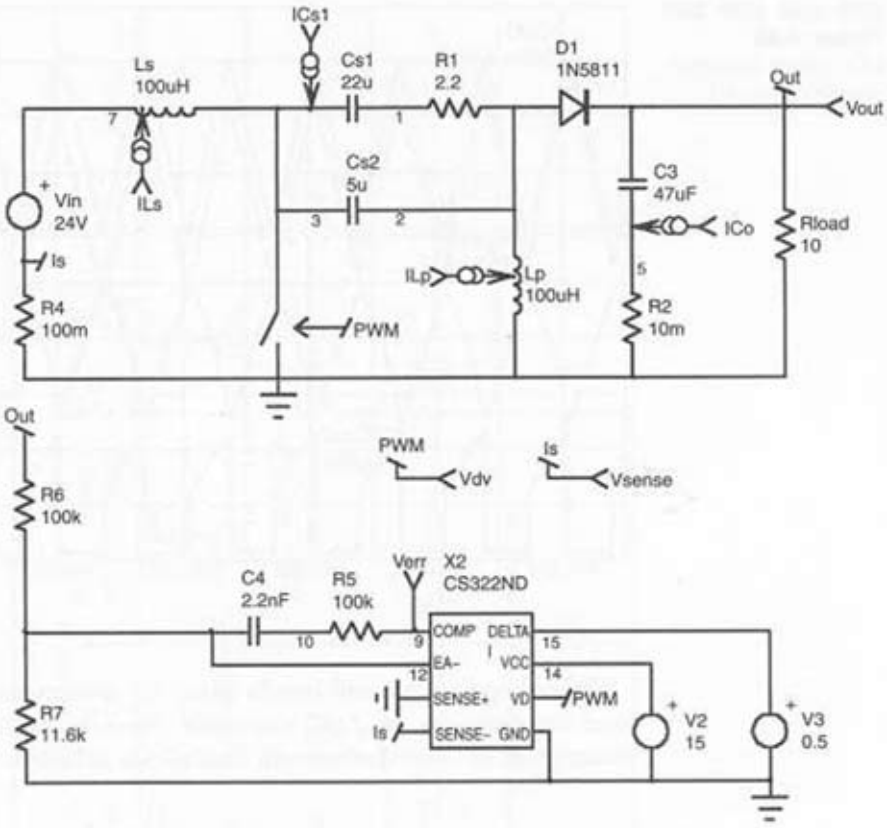


Figure 4-6a
A variable frequency uncoupled SEPIC converter.

The Series-Parallel Resonant Converter

The series-parallel resonant converter, also called LCC, can be implemented by wiring two MOSFETs in a half-bridge configuration (or four in full-bridge) and adding a specific resonating network as Figure 4-8 depicts. Converters using this technique can be designed for *Zero Voltage Switching* (ZVS) or *Zero Current Switching* (ZCS) topologies. Unlike conventional switching devices, resonant converters exhibit low switching losses (if not zero) but are the seat of higher conduction losses due to high RMS current flowing through the semiconductors.

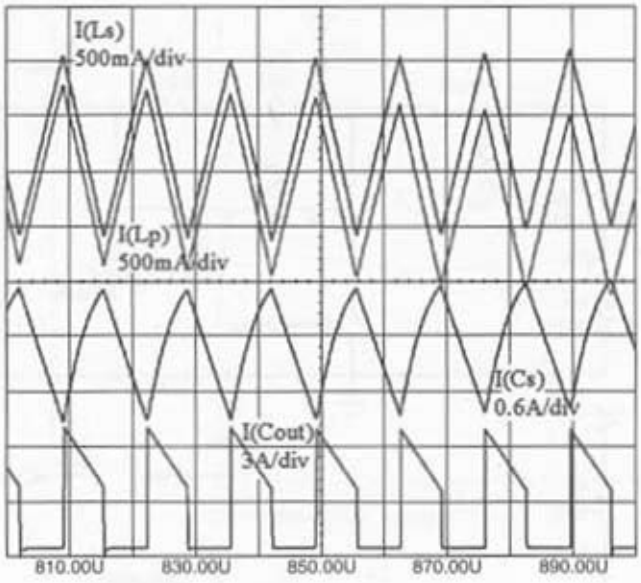


Figure 4-6b
Uncoupled inductor simulation results.

In this section, we will briefly detail an average and a switched simulation template for an LCC converter. Readers interested in a thorough description of these devices will find all the details in reference [21].

Average

The LCC simulation template is based on the series-parallel model developed by Ben-Yaakov and detailed in [28]. All equations are frequency transparent and all the involved values, like current and voltage, are DC in steady-state. They become time dependent during transient steps. The translation process to any platform benefits well from this feature. (See Figure 4-9a.)

In this template, the B1 source plays the role of *Voltage-Controlled Oscillator* (VCO) and transforms the error voltage (across R14) into frequency. Frequency actually corresponds to kV (or kHz) and varies between 100kHz (Verr = 1V) and 500kHz (Verr = 5V). B1 also clamps these values for error voltages outside of this window.

Thanks to the simulation, we easily sweep the output load and see how it affects the quality coefficient of the converter. The loop is being closed in DC by the 1kH, and this operation is greatly simplified because the DC operating point is automatically adjusted. Figure 4-9b details the results.

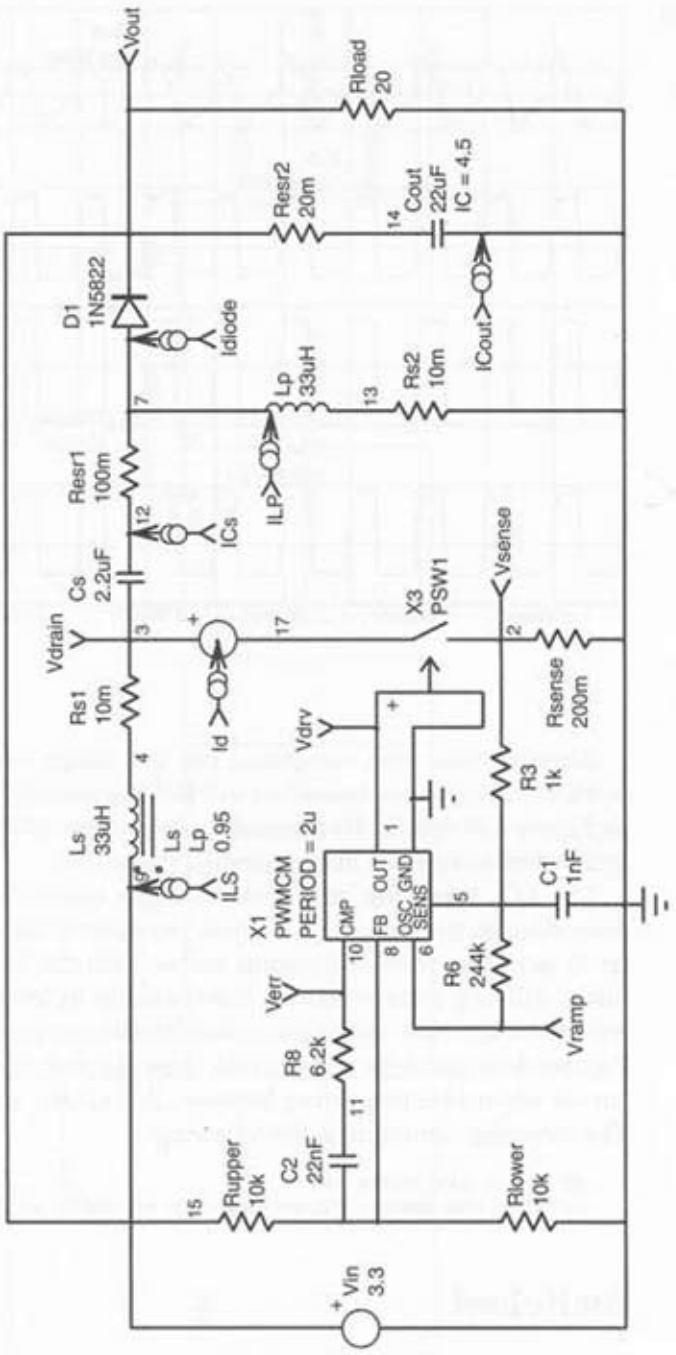


Figure 4-7a
A coupled inductor SEPIC with the current-mode generic model.

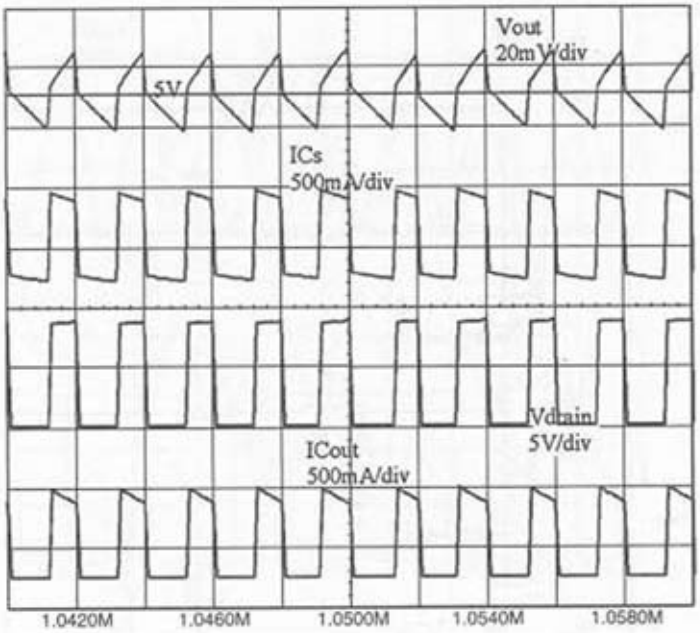


Figure 4-7b
Simulation results show that capacitor Cs current is quasi-rectangular..

Knowing your load variations, you can design your compensating network including worse cases. You will test the stability with a transient step, as Figure 4-9c details. We stepped the input from 300V down to 250V in 1µs and looked at how the loop controlled the output.

The LCC converter can work in either capacitive or inductive mode, depending on the frequency at which you operate. The problem becomes difficult since the resonating point moves with the load; again, the SPICE model will help you circumvent this challenge by letting you sweep the load toward its dynamic range and watch for the corresponding output curves. Figures 4-9d and 4-9e, respectively, show the test circuit and the resulting curves when sweeping Vfreq between 1kV (1kHz) up to 200kV (200kHz). The sweeping command is the following:

```
.DC Vfreq 1kV 200kV 1kV
-->Sweep the source Vfreq from 1kV to 200kV with 1kV steps
```

Switched

Figure 4-10a describes the switching implementation of the LCC converter. There is no generic model, except the dead-time generator, which prevents

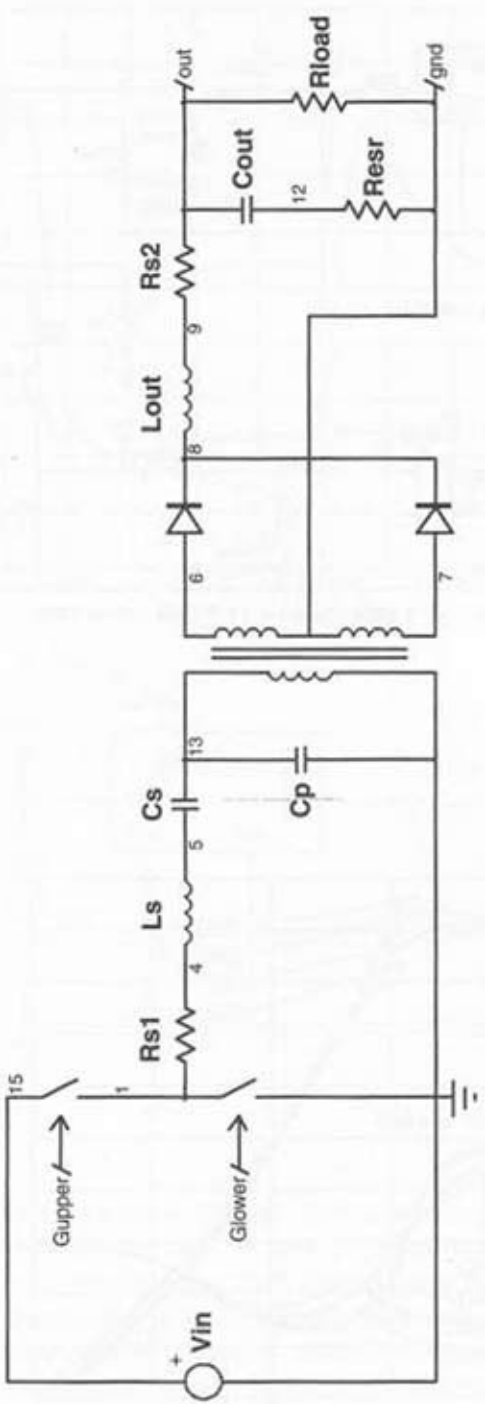


Figure 4-8
A series-parallel resonant converter.

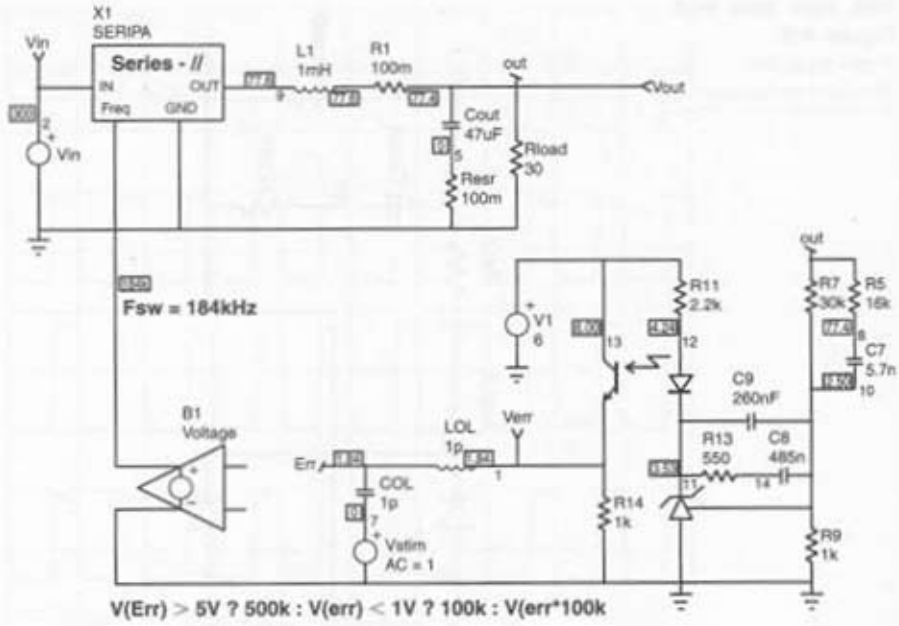


Figure 4-9a
The open-loop LCC average configuration with an error amplifier delivering 200W.

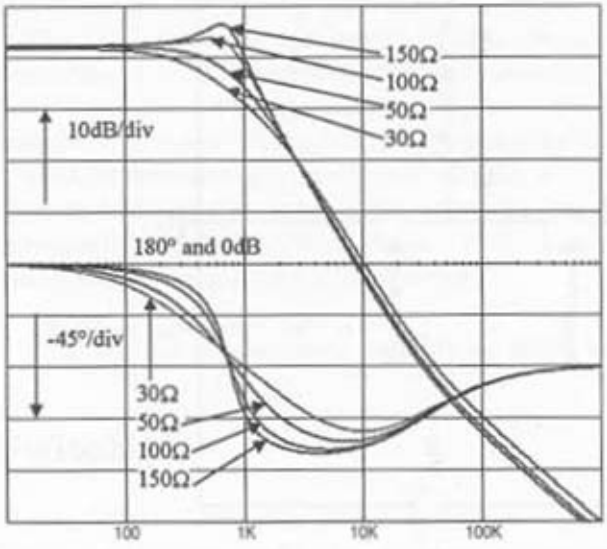


Figure 4-9b
By changing the output load, the Q of the circuit varies and affects the stability.

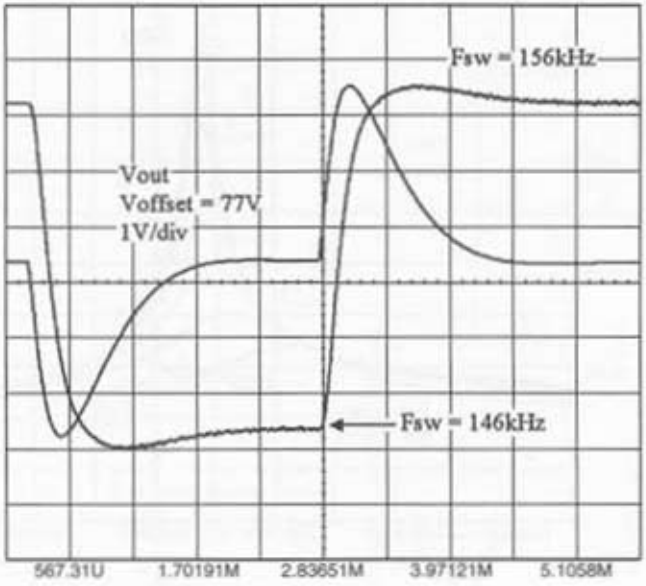


Figure 4-9c
Transient response with RL = 15V.

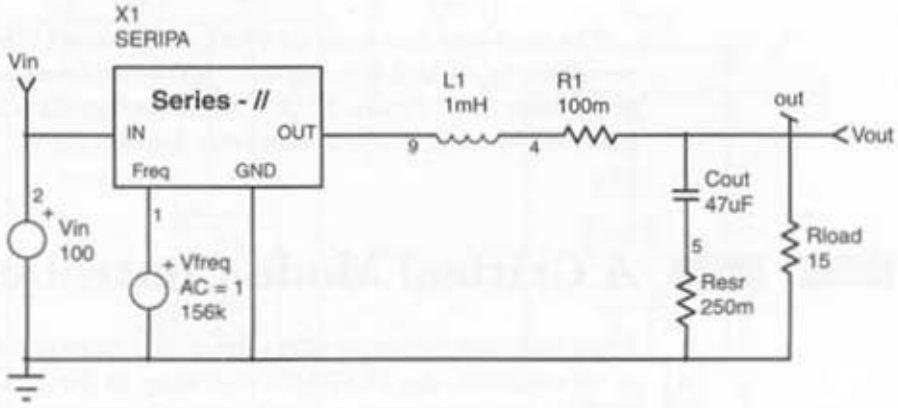


Figure 4-9d
LCC DC gain simulation template with Vin = 100V.

excessive shoot-through. In this schematic, the bottom left section performs the VCO function. It uses a voltage-controlled current source (G1) whose input receives the error voltage, Verr. When Verr is high, the capacitor Ct charges fast and the frequency increases. On the contrary, at low Verr, the frequency is naturally reduced. Once more, the B1 element bounds the switching frequency between 120kHz and 500kHz.

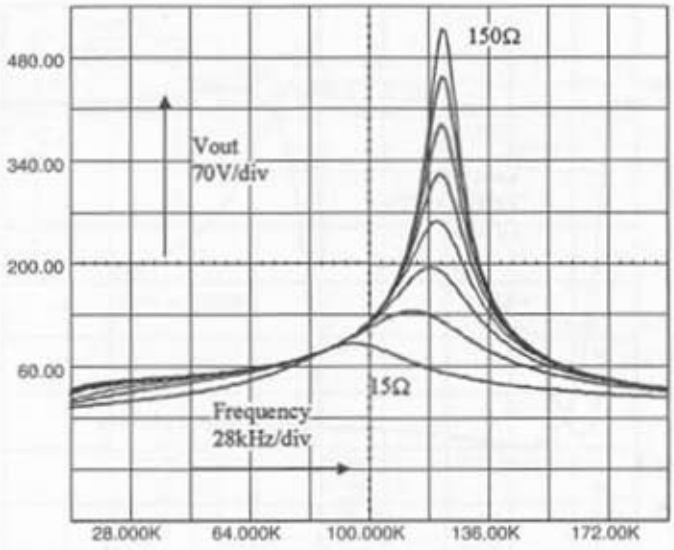


Figure 4-9e
Simulation results with Rload swept from 15Ω to 150Ω.

The dead-time has been set to 200ns. Because of the low bandwidth and correspondingly high time constants, the steady-state level requires a long simulation time. Figure 4-10b depicts the typical waveforms when stabilized. In this case, the LCC converter delivers 200W.

A Critical Mode Controller

If the resonant converter offers the ability to switch at either zero voltage or zero current, the FLYBACK operating in *Borderline Conduction Mode* (BCM) also represents a possible option in very low-cost designs. By delaying the time at which you restart the MOSFET, you can force it to switch in the minimum drain-source region (Vds wave close to zero). Accordingly, this reduces the associated capacitive losses and lowers the EMI content. Some semiconductor manufacturers improperly call it quasi-resonant mode, but valley-switching operation is closer to the reality. Finally, thanks to the forced Discontinuous Conduction Mode, whatever the operating conditions, the system stays a first-order and eases the compensation network design. Figure 4-11a depicts an industrial application using a dedicated controller from ON Semiconductor: the MC33364. This component hosts everything

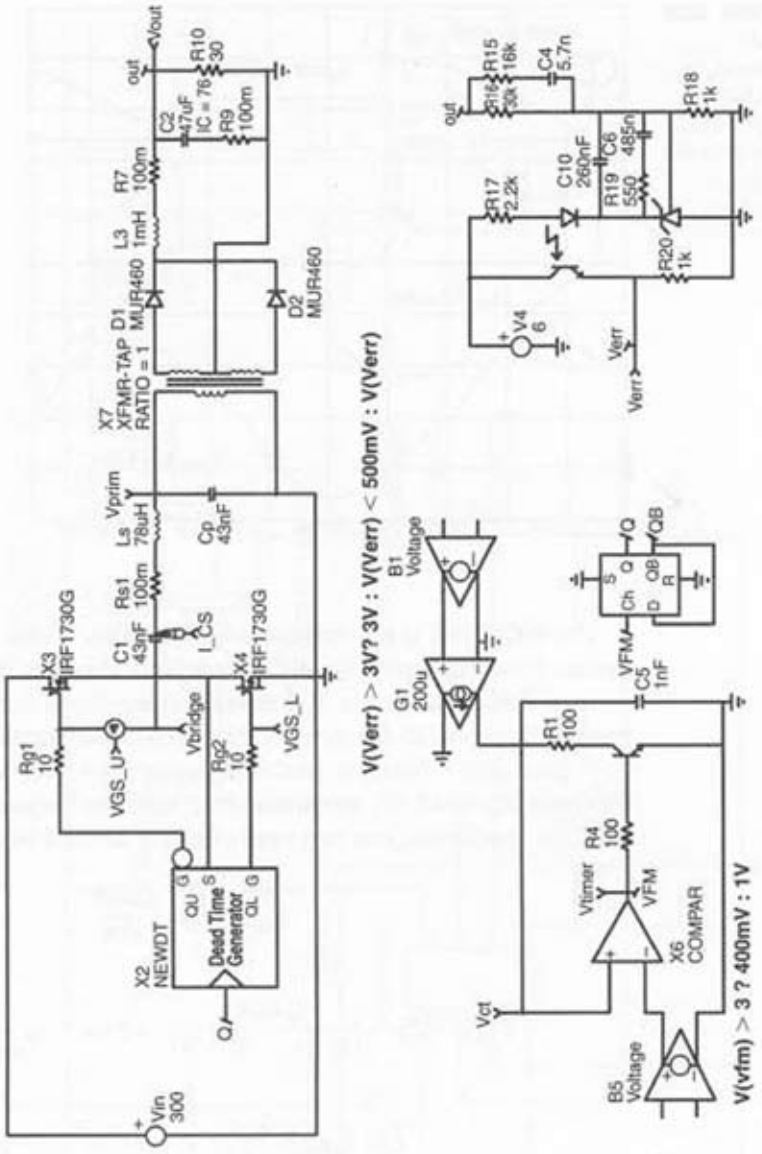


Figure 4-10a
The LCC converter in the switched version includes a complete VCO chain.

needed to build a simple FLYBACK converter working in DCM-BCM. An internal comparator monitors the activity of the core flux through a dedicated winding ($Vaux = N \cdot \frac{d\varphi}{dt}$) and waits until the primary current has fallen down to zero prior to restart the switch.

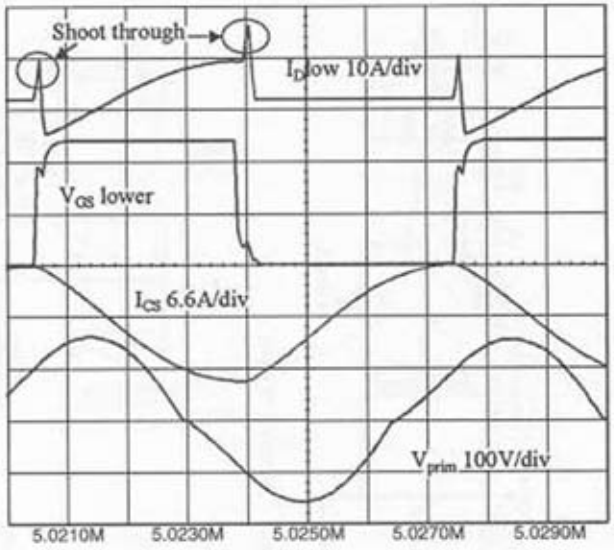


Figure 4-10b
In this simulation, cross-conduction took place. The RMS current flowing in the series capacitor is evaluated to 5.2A.

The MC33364 is a current-mode controller. When the switch closes, the primary current builds up until it reaches the peak setpoint. The FLYBACK voltage then takes place and forces a ramp-down current. As a result, the frequency moves in function of the conditions: The load current increases, Fsw goes down; load current decreases, Fsw goes up until the internal clamp is activated. By understanding how the frequency evolves with load and line conditions, you can easily fix any desired boundaries:

$$T_{ON} = Lp \cdot \frac{Ipeak}{Vin}$$

$$T_{OFF} = Lp \cdot \frac{Ipeak}{[(Vout + Vf) \cdot N]} \rightarrow Fsw = \frac{1}{T_{ON} + T_{OFF}} = \frac{1}{Lp \cdot Ipeak \cdot \left[\frac{1}{Vin} + \frac{1}{(Vout + Vf) \cdot N}\right]}$$

With: Vout the output voltage, Vf the secondary forward drop, Fsw, the switching frequency, Lp the primary inductance and Vin, the input voltage.

Knowing this formula and the maximum peak current fixed by the IC (1V/Rsense, typically), you can calculate the minimum switching frequency you want and thus deduce the value of Lp. With a few more lines of algebra,

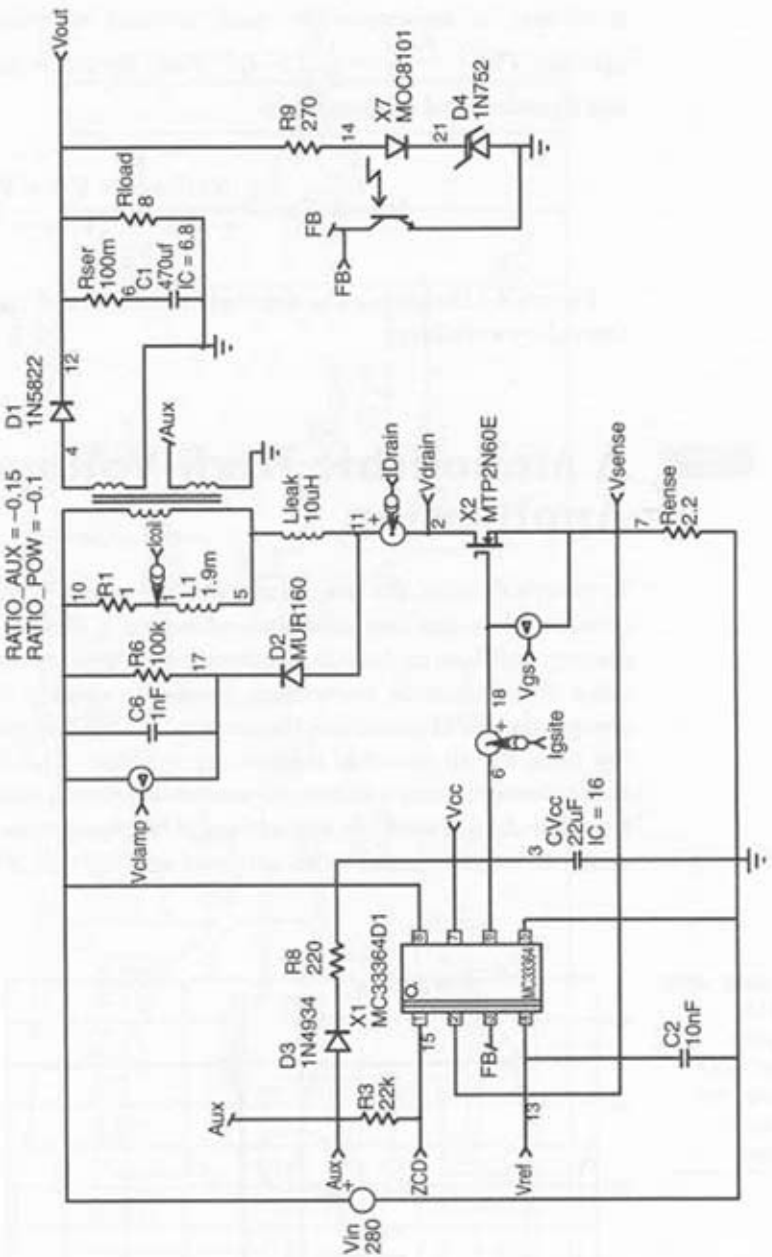


Figure 4-11a
The MC33364 works as a borderline controller.

it is easy to determine the peak current at which the converter will operate: $Pin = \frac{Pout}{\eta} = \frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw$. By replacing Fsw with the previous equation and solving for Ip:

$$Ip = 2 \cdot Pout \cdot \frac{N \cdot (Vout + Vf) + Vin}{\eta \cdot Vin \cdot N \cdot (Vout + Vf)}$$

Figure 4-11b unveils the simulation results and highlights the benefit of the valley switching.

A Monolithic High-Voltage Application

In today's designs, the time to market and ease of implementation are often considered as the key elements preceding a design decision. In this perspective, off-line high-voltage controllers represent an interesting solution since they integrate everything needed to quickly build a rugged SMPS design: the PWM controller, the internal MOSFET, and the startup network (no need for an external dissipating resistor). The MC33363 has pushed these elements into a silicon die and thus offers a ready-to-use offline solution. The device works in voltage-mode but integrates a pulse-by-pulse current limitation thanks to an internal sensing cell. Figure 4-12a depicts a

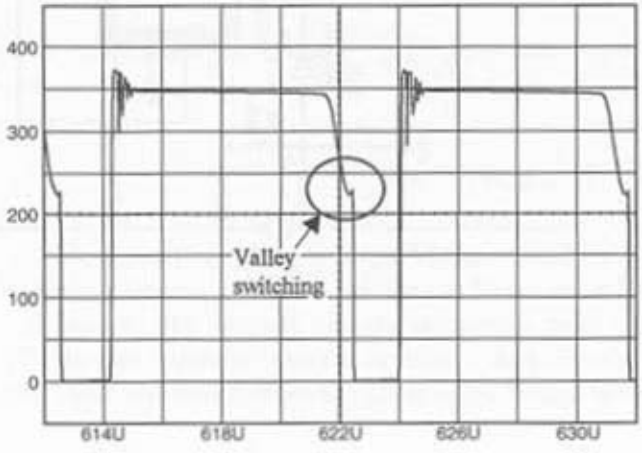


Figure 4-11b
By delaying the switch restart, you can operate in the minimum drain-source region.

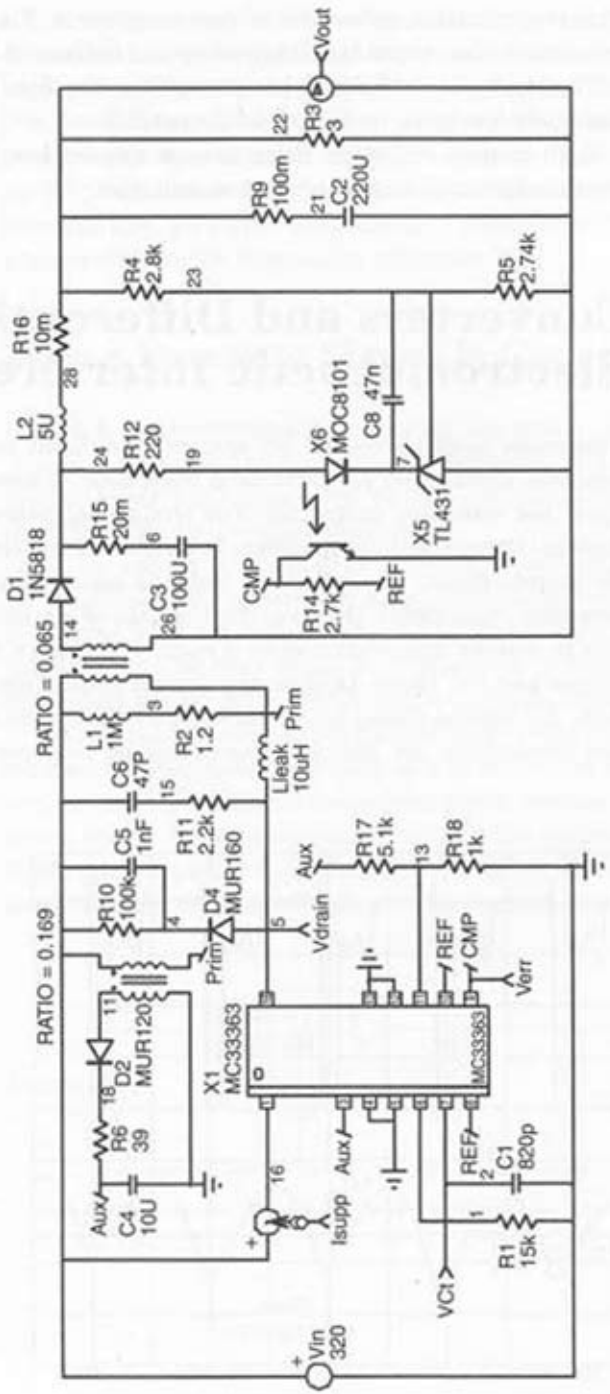


Figure 4-12a
A typical offline application using the MC33363 high-voltage controller.

typical application schematic of this component. Please note that in this simulation, the output is fully floating and delivers 8.3W.

Thanks to an additional low-pass filter, the final ripple is kept at an extremely low level, as Figure 4-12b testifies.

Both models and other discrete ones can be downloaded from the ON Semiconductor Web site at: www.onsemi.com.

Converters and Differential Electromagnetic Interference

If common mode emissions are extremely difficult to predict with simple methods, differential perturbations are easier to assess when you understand the way they propagate. The traditional paper method deals with classical harmonic decomposition. It consists of mathematically describing the current shape, which flows in the bulk capacitor and extracts all of the harmonic amplitudes. However, for the sake of simplicity, the SMPS signature is usually approximated by a recurrent square wave associated with its rise and fall times. Despite the correct estimation given by this procedure, the typical signal delivered by some topologies can be very far from this assumption, for example, depending on the operating mode DCM or

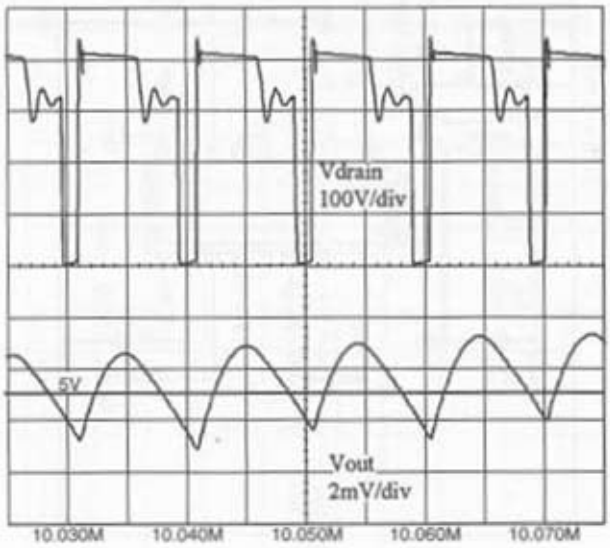


Figure 4-12b
Simulation results of the monolithic FLYBACK controller

CCM. To circumvent this problem, you can precisely calculate the Fourier transform of each original signature and take the worse case for the necessary attenuation. Unfortunately, depending on the external parameters (line level, load, conduction mode, etc), you must perform the calculation for every particular condition. In this chapter, we show how SPICE can do the job for you by analyzing the precise behavior of any particular power structure and then give first assessments of differential EMI results. More information will also be found from reference [35].

How a Parasitic Signal Is Generated

Figure 4-13a represents a simple off-line power supply, regardless of its inherent topology. The transistor is activated by an external *pulse width modulator* (PWM) integrated circuit and chops the current at high frequency inside the primary inductor.

All the energy is provided by the bulk capacitor C_BULK, because of the period difference between the mains and the switching action. C_BULK is recharged at a low rate by the electrical network, and if we consider its impedance to be very small and negligible at high frequencies, then the equivalent model of the whole circuit is shown (Figure 4-13b).

The current flowing inside the inductor is replaced by an equivalent current source whose shape corresponds to the SMPS signature. The capacitor can be replaced with its *equivalent series resistor* (ESR) and, for switch cycles under 1µs, the designer can add the equivalent series inductance (ESL, 20nH typically for a 47µF 400V snap-in). However, one should bear in mind that the equivalent series representation of a capacitor has elements

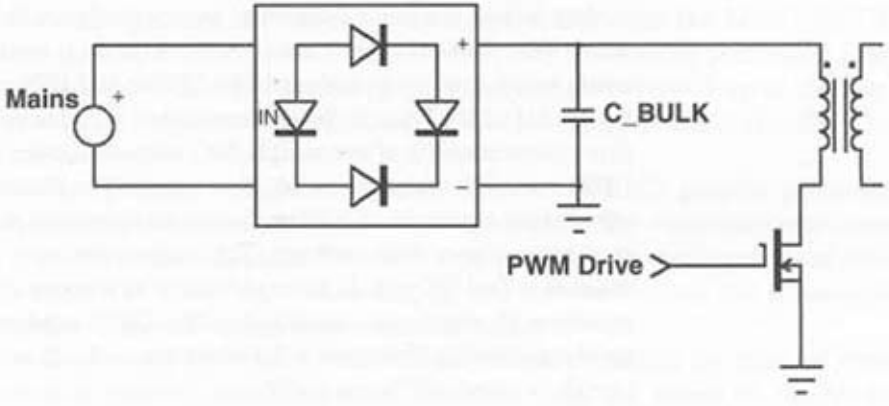


Figure 4-13a
A common structure for low-power offline converters.

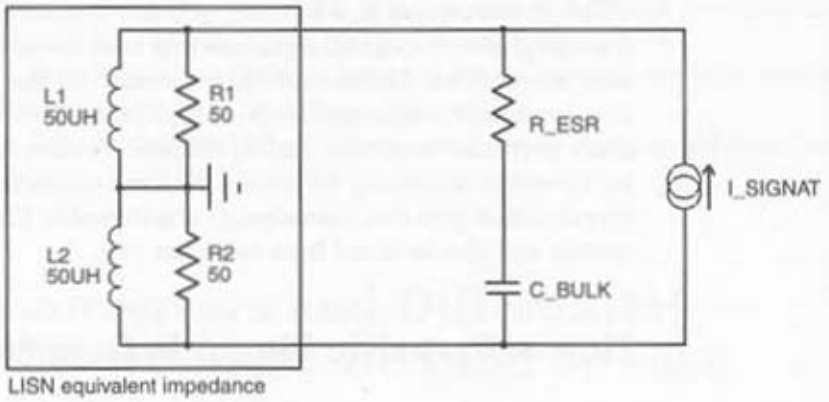


Figure 4-13b
The current signature generates a voltage across the sensing elements.

that are frequency, bias, and temperature dependent. An accurate model should account for all of these contributions although it may be too computationally intensive for some applications. For those who want to include the equivalent series capacitance in their capacitor model, manufacturer C/C_0 curves provide the capacitance value at the operating frequency (C_0 = the capacitance at 20°C and 100Hz). The ESR value can be extracted from the ESR/ESR_0 curves, which depict the variations of this ratio versus frequency (ESR_0 = the ESR at 100Hz and 20°C).

The bridge diodes are assumed to conduct all of the time at these high frequencies and are represented by a short circuit. The final measurement will be carried over a *Line Impedance Stabilization Network* (LISN) as defined by CISPR 16 (Figure 4-13c).

Same Network Declined for Other Phases or Neutral This network is mainly dedicated to (a) maintaining a known RF impedance at the measuring points during a frequency sweep analysis, (b) isolating the device under test from incoming perturbations, and (c) routing the noise components to the spectrum analyzer. The CISPR 16 LISN impedance starts from nearly 5Ω at 10kHz and rises to a constant 50Ω above 1MHz. In our model, this circuit consists of two simple 50Ω sense resistors in parallel with 50μH LISN coils. 5Ω resistors could also be added in series with these coils. By circulating inside the ESR (or the whole capacitor model), the SMPS current generates a noise voltage. This noisy voltage is superimposed on the main rectified DC rail. It then gives rise to a sense signal across both 50Ω resistors. To reduce this noise below the EMC standard limits, the designer needs to install a filter that will isolate the mains from its polluter. The final sketch is given in Figure 4-13d.

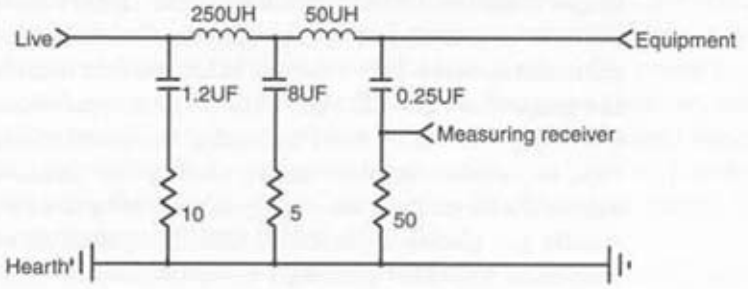


Figure 4-13c
The LISN as defined by CISPR16.

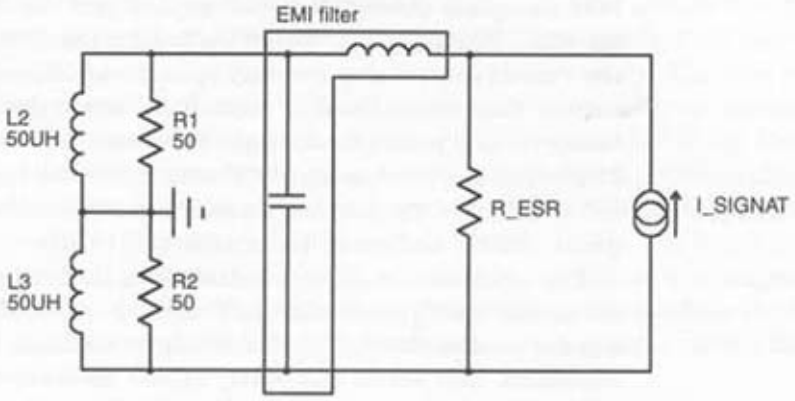


Figure 4-13d
This picture depicts how to wire a differential LC filter before the mains.

Fast Fourier Transforms with SPICE

Rather than manually computing the amount of harmonics present in the current signature (and calculate how they convert into the LISN), SPICE can do the job for you in several ways. The .FOUR directive performs a classic harmonic decomposition over a period and gives results up to the harmonic 10. Unfortunately, you would not be able to graphically visualize the calculations.

Fast Fourier Transform (FFT) function of a SPICE graphic processor usually implements the Sande-Tooke algorithm. The algorithm evaluates the harmonic coefficients from an array consisting of a binary radix of data points (128, 256 . . .). Depending on the software editor, the processing method can differ, as you will discover below.

During the simulation, SPICE continuously modifies its internal time step to provide accurate results. The time step can either be shorter or

longer than the TSTEP variable (in the .TRAN statement), depending on the activities of the computed signals. Generally, the minimum time step cannot drop below $10E^{-9}$ times TMAX, but this boundary also depends upon the proprietary SPICE algorithm. Without specification, TMAX is fixed at (TSTOP-TSTART) / 50. At the end of the simulation, some SPICE simulators, as IsSpice, invoke—before storing the data—a linear interpolation algorithm to produce an evenly spaced output at a TSTEP interval. The results are placed in an ASCII SPICE compatible output file that can be examined with the IntuScope investigation tool. However, IntuScope also offers the capability to explore the raw simulated data.

CADENCE's PSpice does not interpolate the data in its .DAT file. The user navigates through the raw acquisitions via the PROBE graphical interface. When the FFT algorithm is initiated, PROBE first interpolates the data to convert the unevenly spaced acquisitions into fixed time step data. It then places the new acquisitions into a data array of the nearest binary radix of points, for example, 128 locations for a 100-point simulation. PSpice can also produce an ASCII output file with interpolated data points but, in this case, the user must specify the nodes to be saved with the appropriate .PRINT statement in the netlist file (.CIR).

The maximum frequency available from the interpolated data array can not exceed the Nyquist criterion, Fmax = 1 / (2.TSTEP). If higher frequencies are present during the simulation, for example, because of a parasitic oscillation, they would incorrectly appear as lower frequencies when displayed with a graphical interface. Variable time-step simulators like SPICE are equivalent to sampling systems. If the time step becomes too large, aliasing problems will occur and the linear interpolation algorithm will lead to inaccurate results. To circumvent this problem, you should clamp down on the maximum internal time step by setting TMAX to between 1/2 or 1/4 of the TSTEP value. If TMAX is too small, the simulation will be unnecessarily long. If TMAX is too large or not set at all, data aliasing problems can occur.

CISPR16 and SPICE

CISPR16 specifies four measurement bands ranging from 10kHz to 1GHz The bands of most interest to us are bands A (10kHz to 150kHz) and B (150kHz to 30MHz). The standard specifies two different analysis filters to sweep the spectrum from A to B. In range A, the measuring instrument uses a filter whose bandwidth is 200Hz (6dB). In range B, the instrument filter toggles to a 9kHz bandwidth (6dB). Depending on the target compliance curve, the spectrum sweep will be performed with different detectors

types: peak, quasi-peak, or average. For example, the CISPR022 limits are specified for both quasi-peak and average detections, which accounts for weighted charge and discharge-time constants. If the sweep succeeds with a peak detector, it will automatically pass the quasi-peak test, which always delivers a lower output voltage. By modifying the analysis bandwidth during the sweep, the energy encompassed by the filter will change, leveling the noise floor accordingly. Thus, when switching from 200Hz to 9kHz, the noise floor grows by a factor of 16.5dB.

To illustrate this, consider a simulation lasting 100µs in which the user saves the data to an ASCII output file by specifying a TSTEP value of 1ms. This results in 100 data points. When launched under the graphical interface, the FFT algorithm first interpolates the data (except if it has not already been performed) and then creates an array made of 128 locations in which the new interpolated data points will take place. The time interval becomes 100ms / 128 = 0.78ms. With this new time interval, the displayed analysis bandwidth is truncated to 1 / (2 . 0.78ms) or 640.2kHz. Finally, in its time-to-frequency conversion process, the graphical processor places half of the data points in a real array and the other half points in an imaginary array. The result from this example is then 64 points. The frequency resolution is 1 / 100ms or 10kHz. This last value also defines the analysis filter which is centered at 10kHz. Some graphical processors allow the user to build time windows (Hanning, Hamming . . .) in order to reduce the spectral leaks.

Normally, for accurate comparisons between simulated and real plots, the simulation time should be adjusted in order to match the normalized CISPR16 filter bandwidth at −6dB (200Hz and 9kHz). To simplify the various timing values and limit the number of simulated data points, 500Hz and 10kHz will be used as analysis bandwidths.

Analysis Bandwidths

With a SPICE simulator, you cannot modify the time-step resolution accuracy during a transient run. Nevertheless, you can run multiple transients analysis corresponding to the bandwidth you want in separate windows, and then use the copy/paste function upon a common window. The lines below give the SPICE transient commands you can use to obtain various analysis bandwidths:

```
.TRAN TSTEP TSTOP [TSART] [TMAX] [UIC] [optional]
.TRAN 100NS 801US 400US 50NS UIC ; 5.2MHz sweep range, 2.493kHz
analysis BW, 4010 points (5.1)
```

```
.TRAN 24.44NS 500US 400US 12.22NS UIC ; 20.48MHz sweep range, 10kHz
analysis BW, 4091 points (5.2)
.TRAN 489NS 2.1MS 100US 244.5NS UIC ; 1.024MHZ sweep range, 500Hz
analysis BW, 4090 points (5.3)
```

Multiple transient runs can be quite time-consuming. For low switching frequencies (up to 100kHz), a compromise can be found by using a 2.5kHz frequency step associated with a 5.2MHz sweep range. This allows you to quickly run and modify the design.

SPICE Simulates the True Current Signature

We want an exact signature of the power system under test in order to see how the filter diminishes the polluting harmonics. A plot of the target standard displayed over the final waveforms will clearly demonstrate if the calculation failed or succeeded.

Figure 4-14a shows an off-line Flyback SMPS delivering 1A to a resistive load from a 220VAC rectified network. The heart of the circuit is our current-mode generic model that can be replaced by any other equivalent switched model. The supply operates discontinuously. The circuit drives a high-voltage MOSFET whose drain is protected against leakage inductance effects by a clipping network. The current signature is simulated by the controlled current source F1, which routes the primary current into R_ESR and generates the corresponding noisy voltage. The ESR value is taken from the manufacturer's data sheet or through an impedance versus frequency plot. You can even draw the complete ESR + C + ESL network. The rest of the circuit is a direct copy of the previously described model. The final sensed value is extracted from the voltage across RSENS1 and 2 (VSENSE1).

We have adopted the (5.1) command line and run the simulation file. The results are delivered by Figure 4-14b on which we superimposed the defunct VDE871A/B curves, but any template can be drawn (for example, the FCC15A or B or CISPR22). As you can see, the simplified filter made of the 330mH/100nF is not sufficient to filter out the 100kHz fundamental. This kind of filter can typically be implemented using the leakage inductance available from common-mode chokes (≅200-400mH for a 27mH CM choke). If the differential mode is too strong, then either increase the 100nF capacitor (X2 type) to the upper value (220nF) or increase the differential mode inductor. Another solution consists of reducing the switching fre-

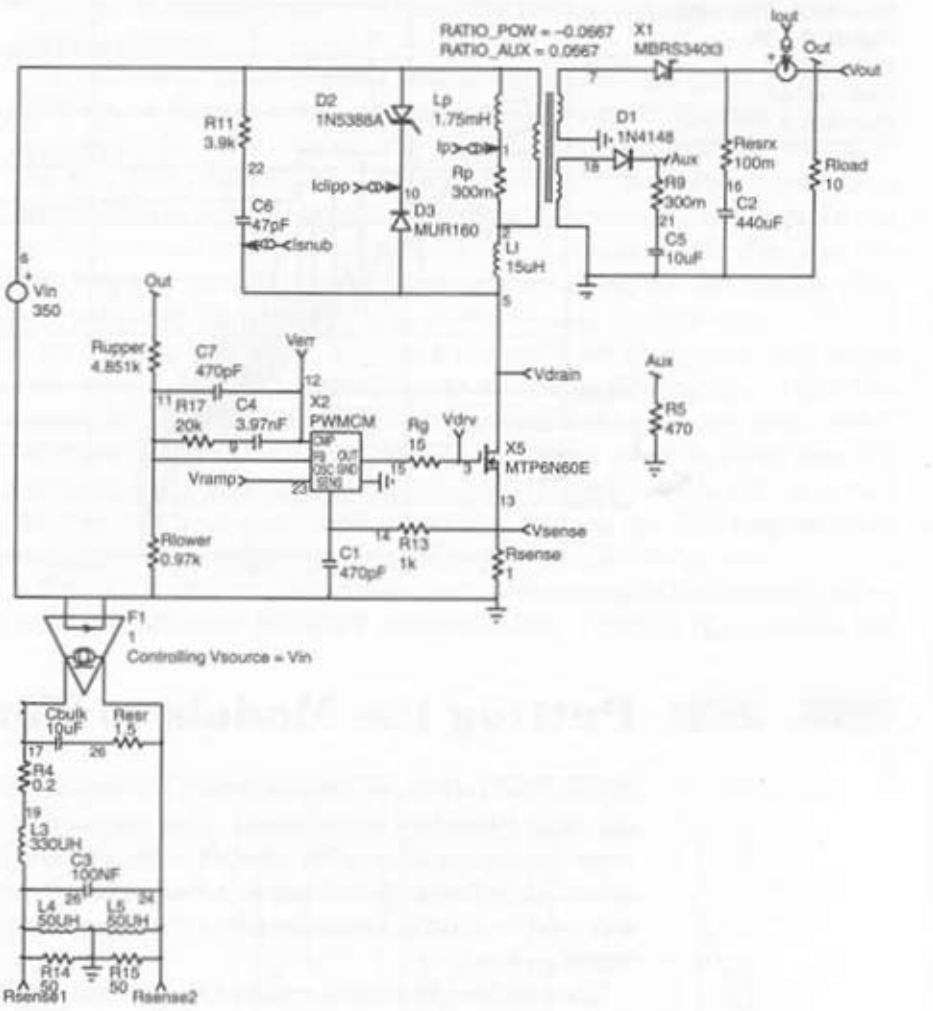


Figure 4-14a
A typical implementation to evaluate the EMI signature of this SMPS—the F1 source routes the power signal into the bulk equivalent network while the 50Ω resistors collect the signals.

quency down to 40kHz to benefit from the natural attenuation of harmonics 2 and 3. This trick is widely used for low-power offline battery chargers.

To display dBmV, simply convert the sensed signal into dBV (20.Log(Vsense1)) and add 120. By doing this, you obtain dBµV (0dBµV = 1µV, 60dBµV = 1µV, etc. . . .).

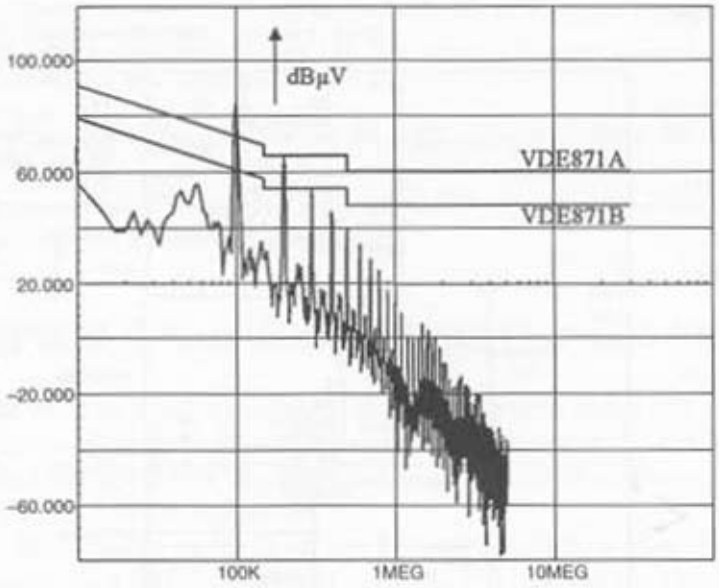


Figure 4-14b
The resulting spectrum when operated at high line.

Putting the Models to Work

In this final section, we are comparing the results delivered by SPICE versus true laboratory experiments. This comparison phase is mandatory when developing models. We selected an MC44608 design (a bit like the one described in Figure 3-25a) but in a true switched version. The demoboard was used for practical measurements of leakage effects, drain-voltage waveforms, and so on.

The leakage inductance creates a sharp voltage spike at the switch opening. To prevent a lethal drain excursion, a clamping network needs to be put in place. We selected an RC type, but an active circuit made of a transient suppressor could also be wired. The simulation is interesting because it will reveal the final steady-state value in overload or startup conditions. The RC types are particularly sensitive to the peak current; the maximum voltage excursion shall always stay within safe limits even at the highest Ipeak. If for any reason the clamping level goes beyond the limit you expected, the SPICE MOSFET stays alive, a good advantage of SPICE simulations! The results are shown in Figure 4-14a and 4-14b.

The overall shape is in good agreement with the real data. However, the average level is slightly higher in the simulated graph. This could come

from a small mismatch between either the leakage inductance or the working peak current.

Steady-state values are also interesting to evaluate peak, average, or RMS values. Figures 4-15a and Figure 4-15b, respectively, show the simulated drain variables (voltage and current) compared with the real data. The duty-cycles are very close to each other (22%), but differ slightly from the value given by the averaged simulation. This variation can be explained by the presence of the primary leakage inductance, which degrades the open-loop gain by delaying the primary to secondary current transfer. The error amplifier fights this effect by strengthening the duty-cycle.

By the same philosophy, Figures 4-16a and 4-16b show the overall shape of the secondary rectifier current when delivering 52W at Vin = 120V. The supply has already entered CCM, as demonstrated by the step at the end of the pulses. The differences between the peak value might be found from the discrepancies of operating frequency (100kHz with SPICE, 96kHz in real life), but also from other ohmic losses that degrade the open-loop gain and force a higher primary peak current to stabilize the output level.

The latest data will depict the current circulating in the leakage inductance just after the MOSFET switch-off time. Figure 4-17a presents the

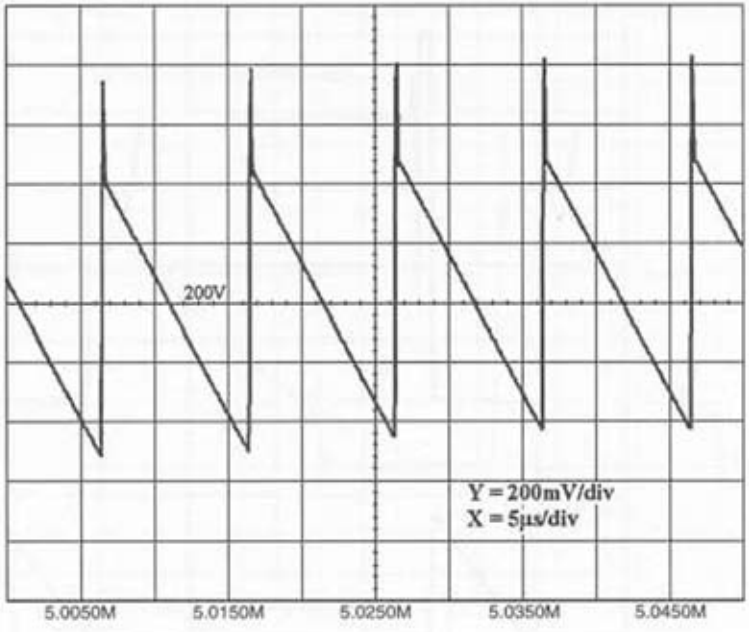


Figure 4-15a
Simulated ripple over the 200VDC clipping level.

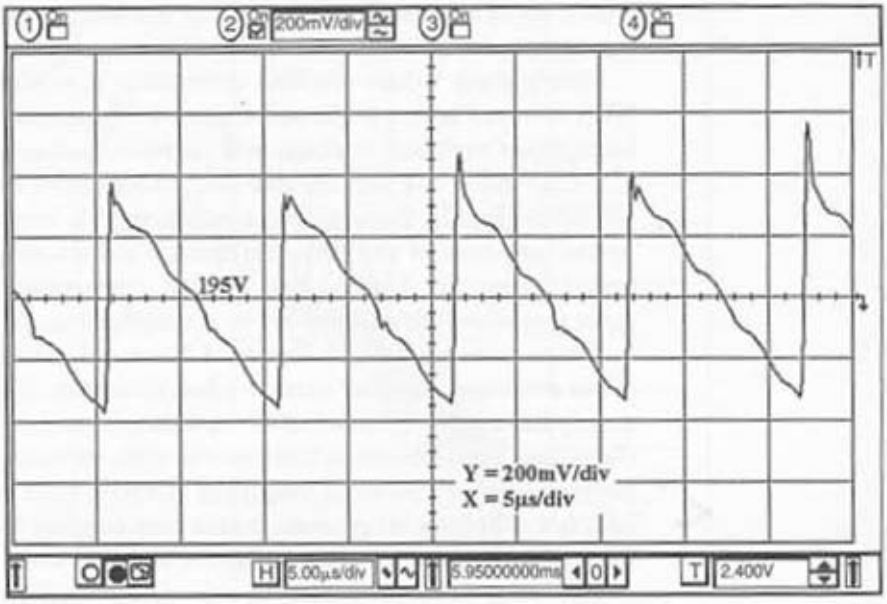


Figure 4-15b
Real measurement of the ripple level at Vin = 120VDC.

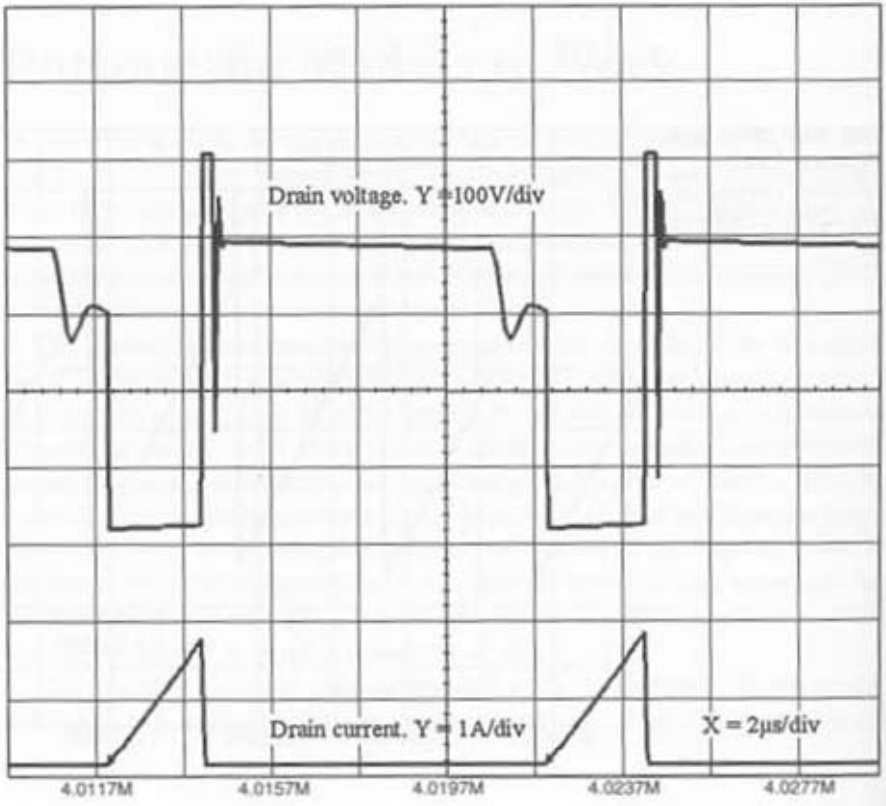


Figure 4-16a
Simulated drain voltage and current at Vin = 282V.

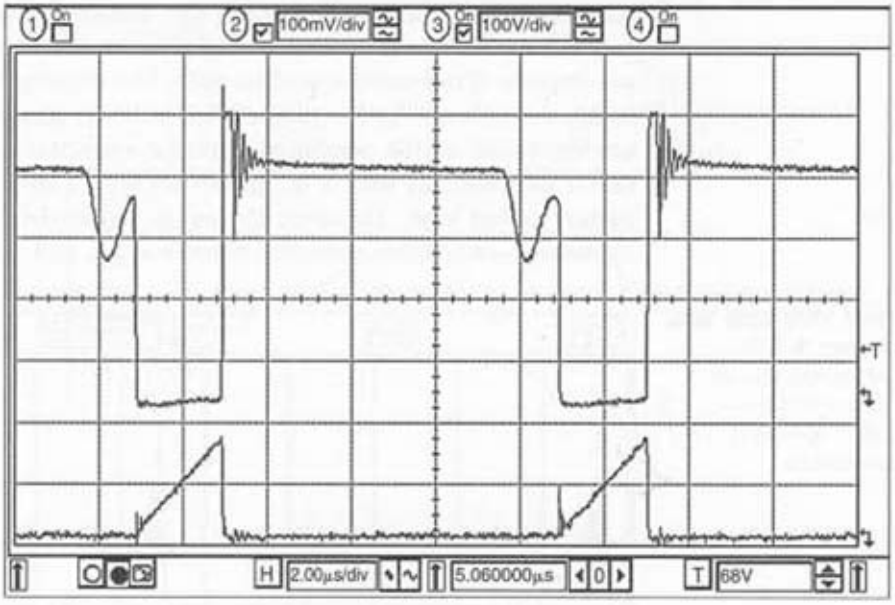


Figure 4-16b
Measured drain voltage and current—same operating conditions.

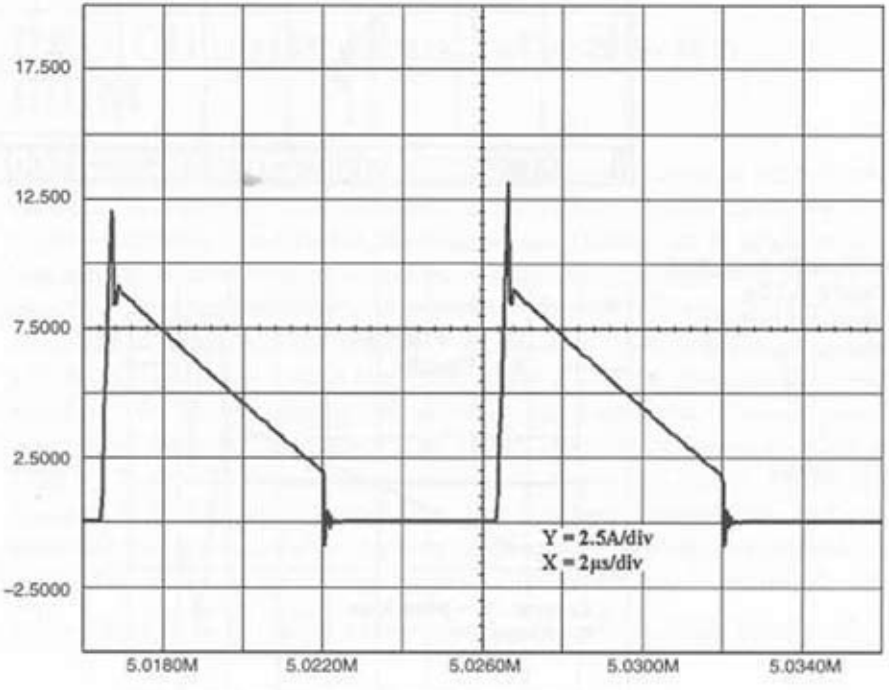


Figure 4-17a
Simulated secondary rectifier output current at Vin = 162V.

results, while Figure 4-17b depicts the real data. The first comment concerns the peak current, which is higher in reality, confirming the previous assumption of degraded open-loop gain. The clipping level is in good agreement, as confirmed by the plateau on the drain waveform. The oscillations are the result of the combined parasitic capacitances, unfortunately not taken into account with a simplified MOSFET model (voltage-controlled switch in this case). However, the simplified model allows for a dramatic increase in simulation time (see Figures 4-18a and 4-18b.).

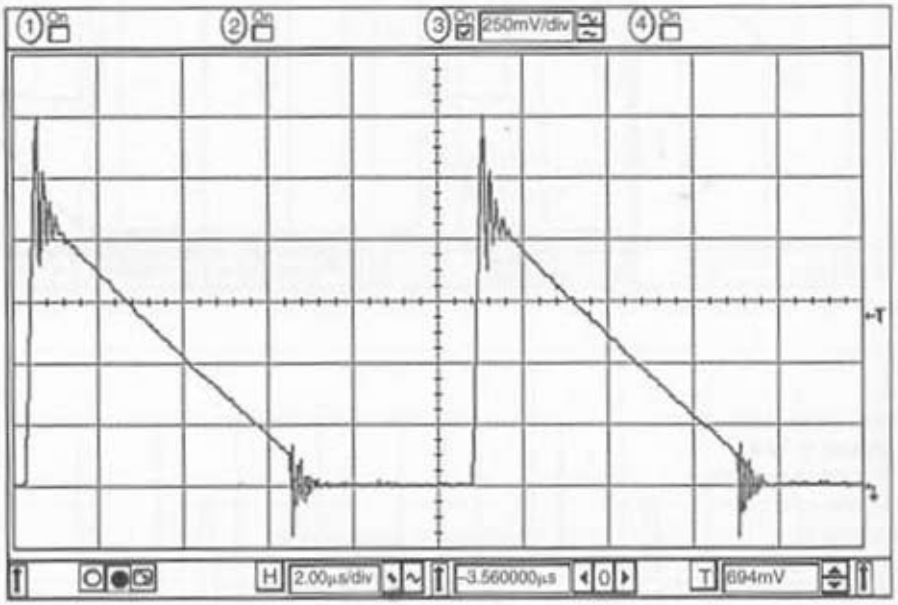


Figure 4-17b
Measured output power rectifier—same operating conditions.

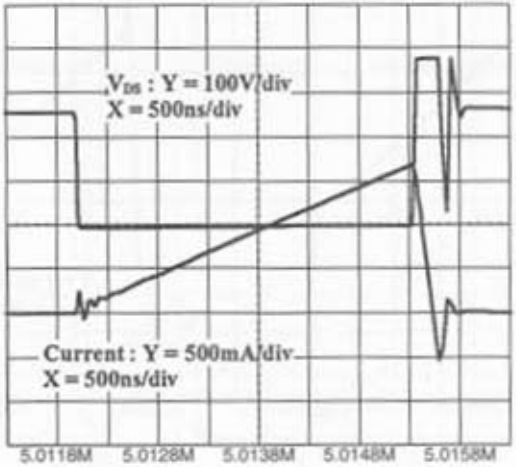


Figure 4-18a
Simulated primary leakage current at Vin = 182V.

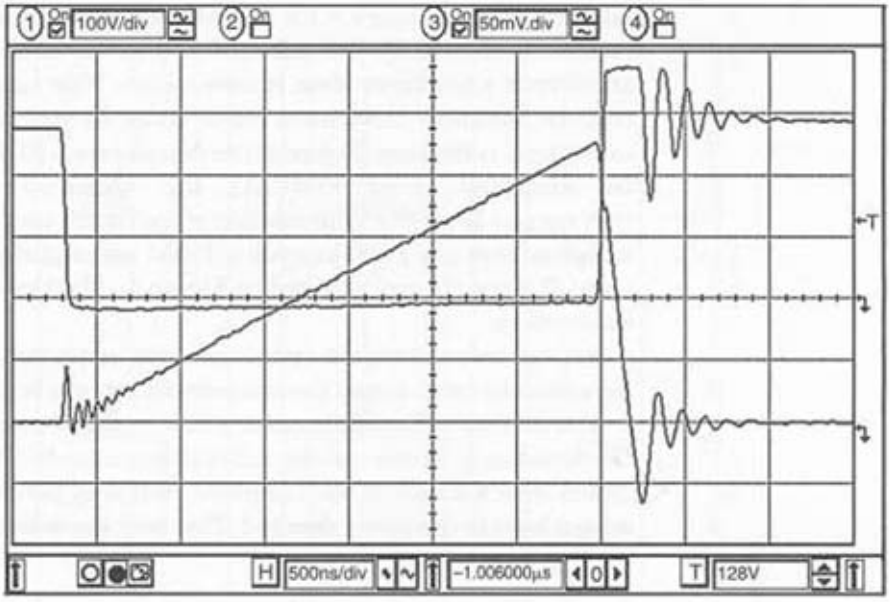


Figure 4-18b
Measured primary leakage current—same operating conditions

PFC Circuits Simulation with PSIM

As we have already explained, SPICE continuously adjusts its internal time-step to cope with the fast current or voltage transitions occurring during the simulation. As a result, the computational time can be prohibitively long when you need to observe low-bandwidth response time switching at a high frequency, typically, *Power Factor Correction* (PFC) circuits. If you can successfully simulate a PFC with SPICE, the amount of data the simulator will finally generate makes the final study a painful process. To better simulate this kind of circuit, we strongly encourage you to use a power electronics-dedicated simulator like PSIM, released onto the market in 1993 by Powersim Technologies, a company based in Canada. PSIM, the opposite of SPICE, keeps a fixed time step during the simulation and considers all the elements perfect having no associated conduction or switching losses. For instance, the voltage generated by inductance is commonly calculated by $e = L \cdot \frac{di}{dt}$. After a discretization procedure, PSIM finally calcu-

lates the voltage using $e = i \times Req$ where Req corresponds to an equivalent resistor evaluated by the software at a given time. When the simulator encounters a nonlinear zone, it uses a Piece Wise Linear algorithm, which cuts the nonlinear behavior in linear slices. As you can imagine, the simulation time is flashing. Figure 4-19a details how a FLYBACK converter can be simulated using SIMCAD, the dedicated schematic capture.

A normal 3ms SPICE simulation of the circuit took nearly 10 minutes to complete over our P350 computer. PSIM accomplished the work in 4 seconds! The results are delivered by Figure 4-19b; they detail the classic parasitic effects.

As you can see from the application schematic, you need to add all of the parasitic elements across the components you use because they are perfect.

The PFC we will simulate uses a new concept recently introduced by ON Semiconductor known as the follower-boost mode. This topology actually differs from a standard boost implementation by permanently adjusting the output level to the power demand. That way, the delivered voltage no longer

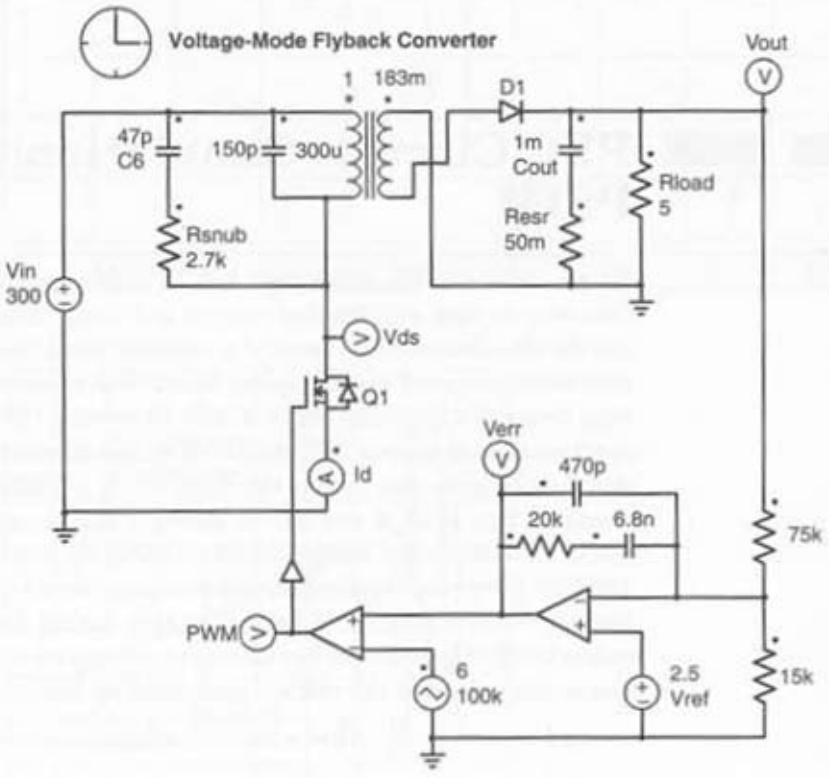


Figure 4-19a
A user-friendly interface allows a quick schematic capture.

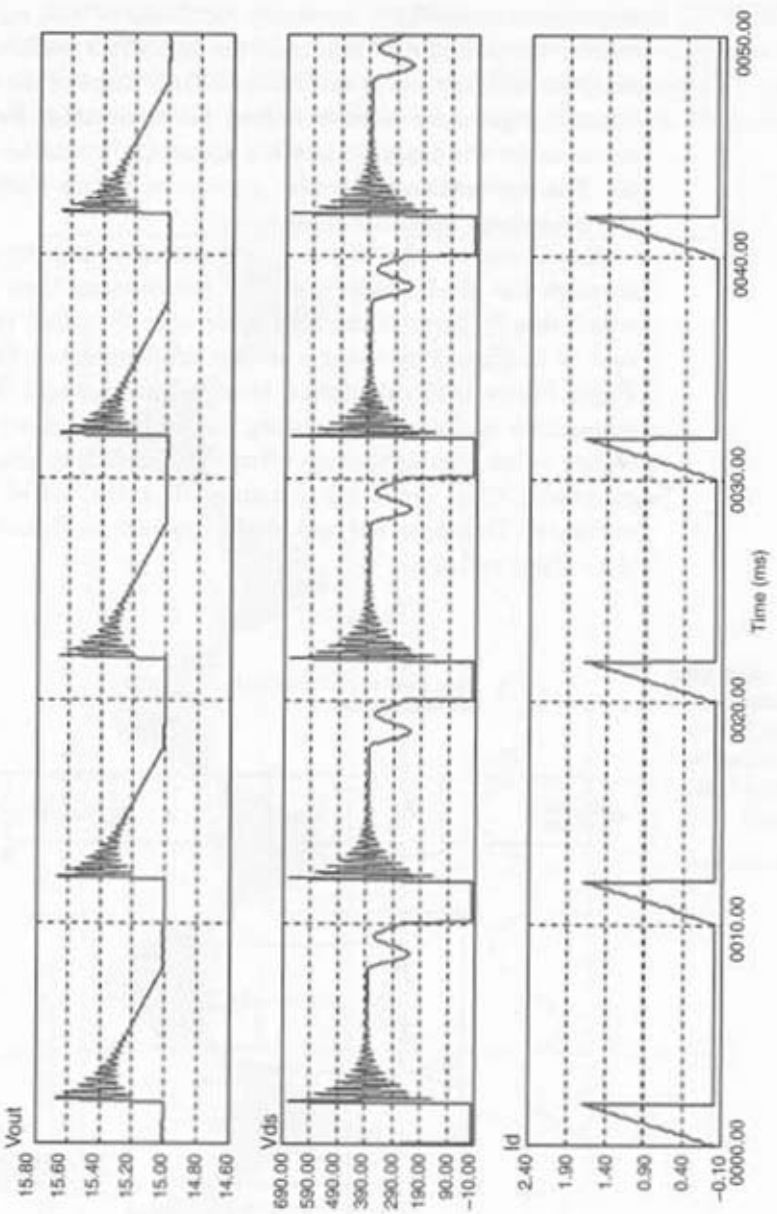


Figure 4-19b
PSIM results can be easily displayed using SIMVIEW.

stays fixed at 400VDC as usual, but "follows" the mains level and varies with the load. To fulfill this task, the MC33260 feedback loop implements a feedback information proportional to the square of the output voltage. Thus, you no longer need to adopt higher voltage ratings for your supply components as for the traditional 400V approach; a smaller inductance does the job. The application schematic is given in Figure 4-20a and corresponds to the data-sheet application example.

As you can see, the IC senses the output voltage by monitoring a current through the R1-R2 network. This information then follows a given law, which finally governs the duty-cycle over the main period. The input current is displayed by using a dedicated Ampmeter. You could also place a *Power Factor* (PF) calculation block, which delivers the PF value once the simulation is done. By changing the input frequency from 50/60 Hz to a higher value, you further speed up the simulation time. In the example, we selected 200Hz, which led to a simulation time of 15 seconds on the P350 computer. The input current shape appears in Figure 4-20b together with the output voltage.

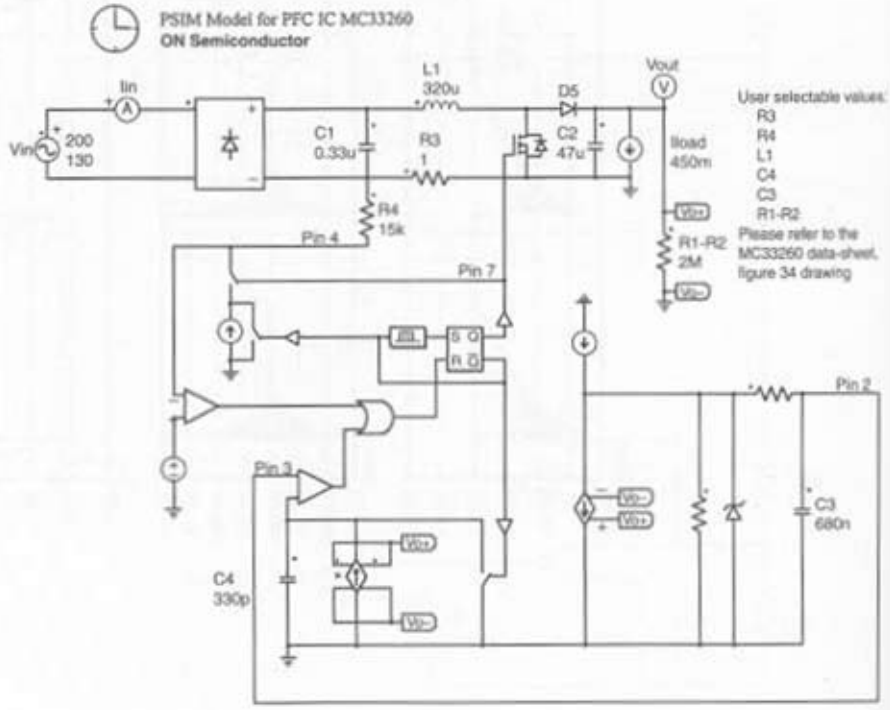


Figure 4-20a
The PSIM MC33260 application example describing the new follower-boost principle

The PSIM demo version is available on the included CD-ROM and contains numerous working application examples. You will find another template with the MC33261 file: the first ON Semiconductor PFC generation. The Powersim Technologies Web site address is given in Appendix C.

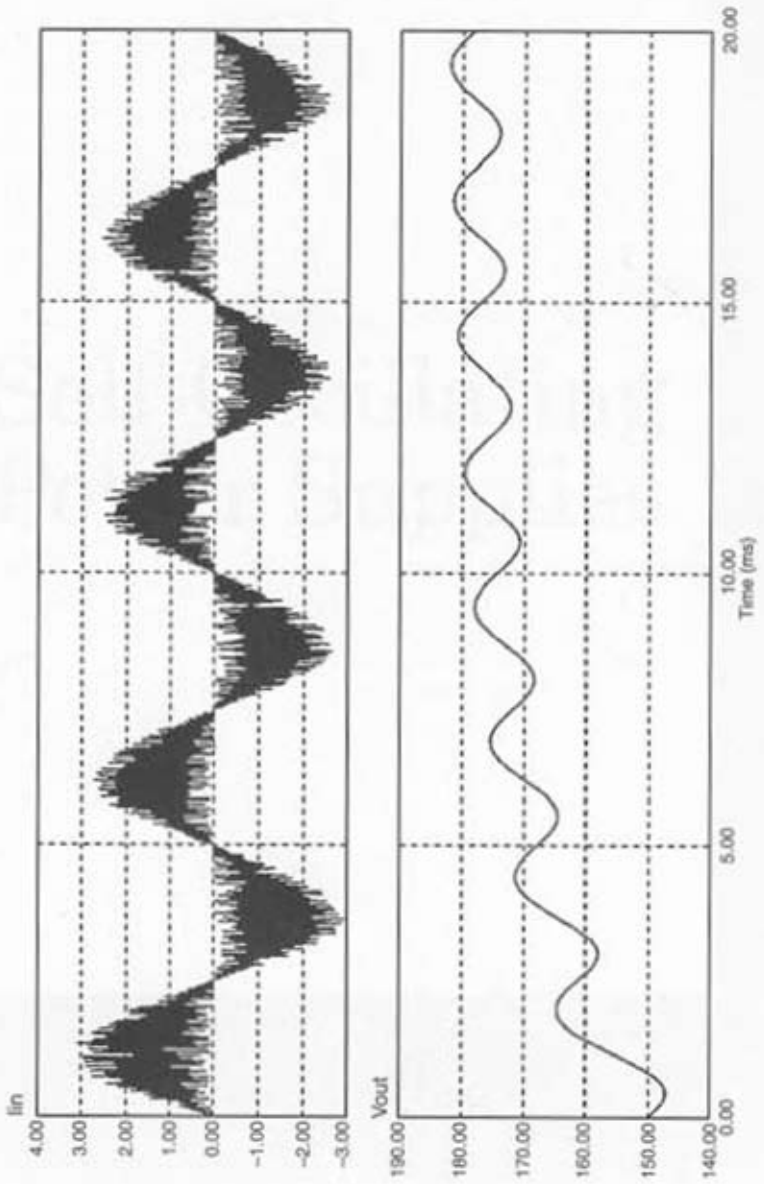


Figure 4-20b
Simulation results obtained after 15 seconds of simulation time.

CHAPTER 5

Self-Oscillating Power Supplies

In the quest for the lowest product cost, designers strive to reduce as much as they can on the number of components used for their Switch-Mode Power Supplies. If building an SMPS around a few bipolars and a MOSFET offers reasonable performance, it clearly suffers from the difficulty to cope with the absence of load, one of the obvious drawbacks. However, applications exist where the load is rather constant, that is, standby or auxiliary SMPS, and the self-oscillating power supply represents a good candidate. We will study two different concepts: one where the device implements a saturable transformer (the good old blocking . . .), and another where the relaxation is made through speed-up pulses. Please note that for translation reasons, these examples will only be available under IsSpice4 at the time this book is printed.

The Good Old Blocking . . .

The blocking was introduced at least 30 years ago, when television sets where sweeping the screen horizontally with a single high-voltage transistor. Figure 5-1a depicts a typical configuration for a blocking oscillator.

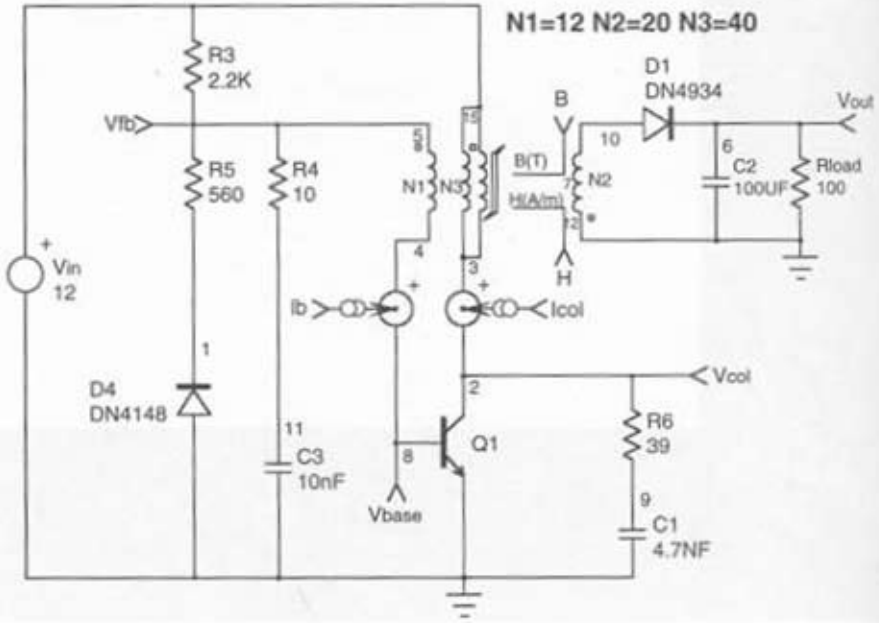


Figure 5-1a
A typical blocking oscillator made with a single transistor.

At power-on, Q1 is biased through R3 and N1 winding in series. As a result, Q1 immediately conducts and applies Vin across N3. No output energy transfer takes place because we are in a FLYBACK configuration (N2/N3 dots are in opposite positions). However, thanks to the dot arrangement between N1 and N3, Q1's conduction is reinforced as soon as the collector current Is starts to rise. This collector current creates a flux that in turn creates a voltage over N1: $V = N \cdot \frac{d\varphi}{dt}$. This further biases Q1 (with the help of D4 and R5, which limits the base current). Ic now grows up until the transformer saturates. The gain β of a bipolar transistor depends on its collector current. If this collector current exceeds a certain limit, the gain starts to fall. This actually happens in the circuit thanks to the transformer's saturation; the total permeability μr.μo collapses to μo and the primary inductance vanishes, engendering a rapid collector current increase. Now, b starts to bend; the primary flux changes its slope from positive (Ic rising) to negative (Ic falls down). The voltage across N1 becomes negative (2df) and now blocks Q1. As in a normal FLYBACK, the primary current transfers to the secondary and Vout increases. Another cycle can take place when C3 releases Q1's base. For peak current less than 2A, ON Semiconductor MMBT589 could be a good choice for this application.

The saturation transformer is made of a perfect transformer associated with a material model (as described in Chapter 2 "Generic Models for Faster Simulations"). Many ways exist to model a ferrite material; reference [27] offers an interesting review. We have, however, stuck to the generic INTUSOFT's approach as described in the IsSpice4 reference manual (also in [27]). The IsSpice4 reference manual details how to extract the parameters particular to a given core.

Figure 5-1b depicts the resulting B/H curve when the converter is stabilized.

Simulation Results

Figure 5-1c gathers some typical waveforms, among which you will recognize the collector current with the typical transformer saturation effect. The delivered power is around 2.5W. Less power can be obtained by increasing R5.

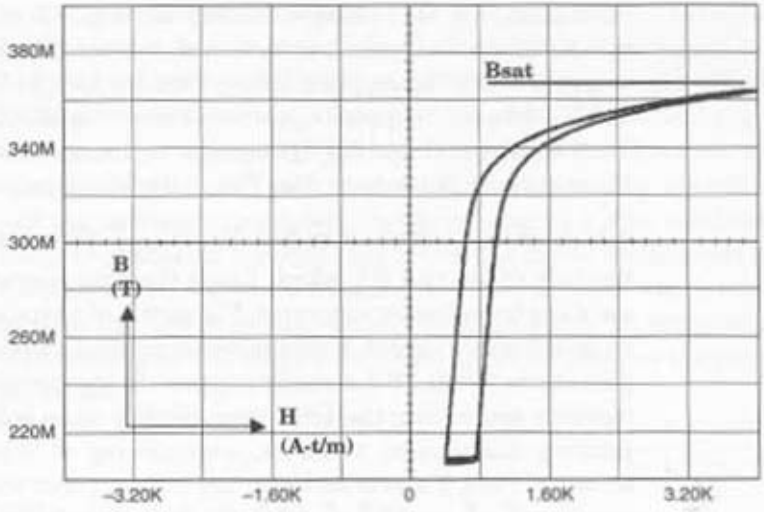


Figure 5-1b
Once the saturation is reached, the material permeability μr drops.

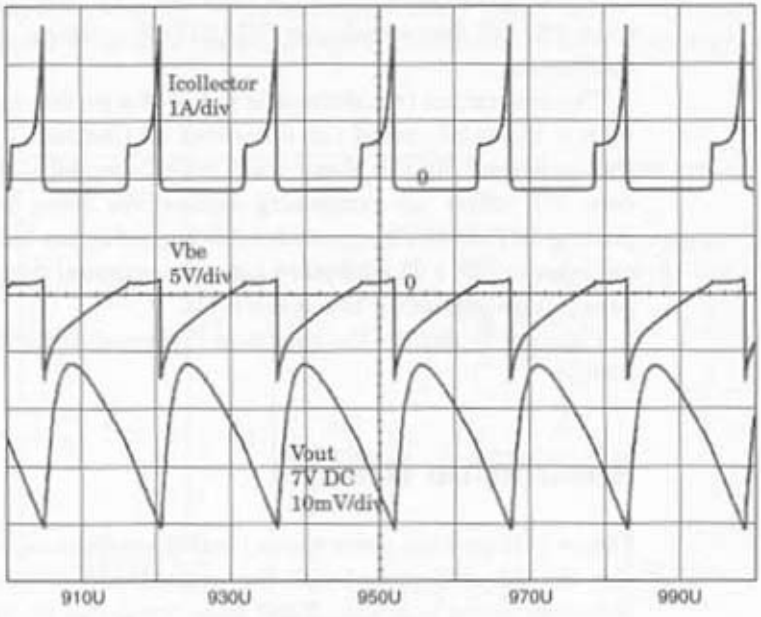


Figure 5-1c
Operation of the blocking converter with a generic saturable transformer.

Self-Relaxing Power Supply

Without using a saturable transformer as before, it is easy to build a self-relaxing power supply. The idea is to use a discrete thyristor to block the main switch when the maximum peak current has been reached. Figure 5-2a describes this concept.

As was the case with the blocking example, we need a regenerative turn on. That is to say, when the main switch is asked to be closed, some external signal shall force it to actually stay closed. This effect is accomplished through the speed-up pulses delivered by the auxiliary winding at node Auxiliary. Operated in FORWARD, the Auxilary winding applies N.Vin when the switch closes and strengthens the gate command. When the primary current is reached, the Q1/Q2A thyristor fires and stops the MOSFET's conduction. As in any FLYBACK converter, the primary-to-secondary

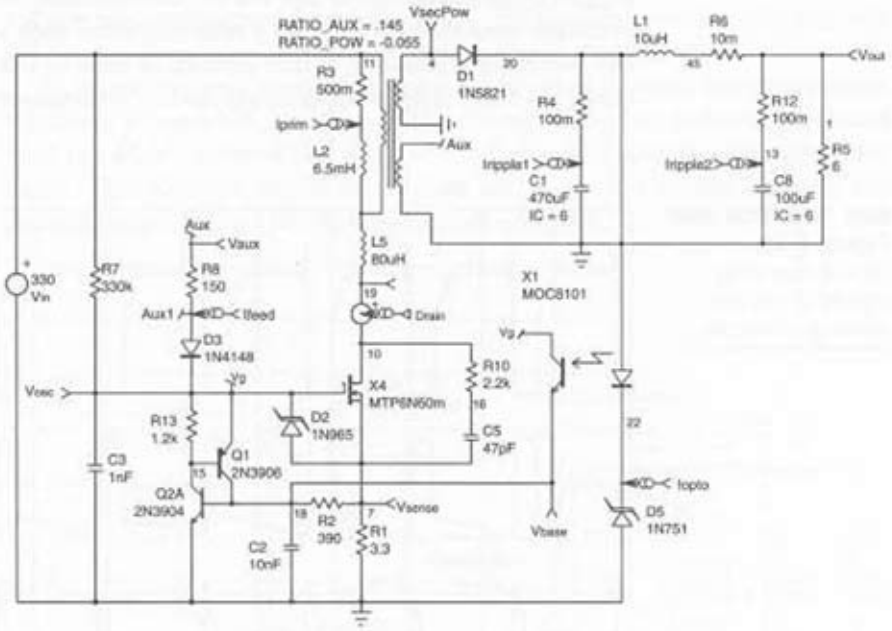


Figure 5-2a
A fully regulated self-relaxing SMPS.

energy transfer now takes place. The regulation is finally obtained by shifting up (Pout demand decreases) or down (Pout demand increases) the current sense information over C2. This prototype has been tested and given a 70% efficiency at 120VAC input voltage. Be careful because in this configuration, the converter does not like to be unloaded (See Figure 5-2b).

Electronic Ballasts

Bipolar Version

Self-oscillating electronic ballasts are very popular in either industrial applications for high-output powers (150W and above) or in domestic use through *Energy Saving Lamps* (ESL). Despite the introduction of dedicated high-voltage drivers, self-oscillating devices are still in use thanks to rugged bipolar transistors like the BUL series from ON Semiconductor. The principle consists in supplying a resonant tank with a 50% square wave. If the switching frequency of this pattern is close to the tank resonating frequency, a high voltage appears across the fluorescent tube terminals. Pro-

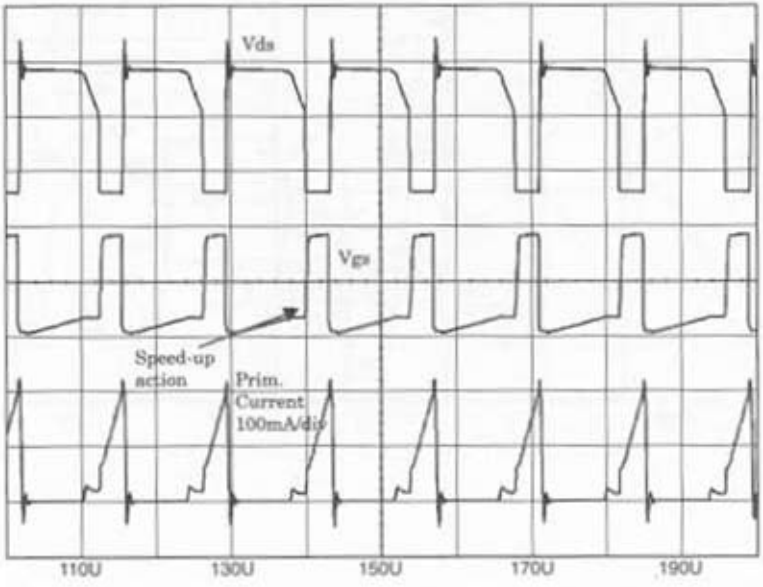


Figure 5-2b
Typical operating signals of the self-relaxing converter.

vided that the voltage is large enough, the lamp strikes. By striking, the tank-quality coefficient is severely damped and the tube voltage drops to its steady-state value. Because the lamp incremental resistance is negative once struck, it necessitates a ballast element for stabilization of its operating point (like in classical mains-operated magnetic ballasts). This is L1 in our schematic, but thanks to a rather high switching frequency, its size and weight are negligible. The striking action uses a voltage-controlled switch offering a given ON resistor (220V in our example for a 40W lamp).

As Figure 5-3a testifies, two transistors and a DIAC are enough to build a complete converter. The operation is very similar to that of the blocking in the sense that the main transformer saturates when a large current flows through it. The idea behind the structure lies in transistors being self-driven by their own winding; if the upper transistor Q1 conducts, the collector current gives birth to a voltage over N1 and actively maintains Q1 biased. Because of dots' position, a positive voltage on N1 gives a negative voltage on N2, which blocks Q2. However, when the transformer saturates (not L1), the flux slope becomes null and reverses: $N \cdot A \cdot \frac{dB}{dt} = 0$. As a result, N1 voltage also reverses and now blocks Q1. N2 becomes positive and can bias Q2 for another cycle until the saturation flux is reached again.

At power on, both transistor bases are shorted through their respective windings N1 and N2. Thanks to C12's charge, a start-up pulse is generated with the DIAC network (D13/14), which furtively biases the low-side transistor. This element starts to conduct and pulls the bridge node to the ground, engendering the aforementioned scenario.

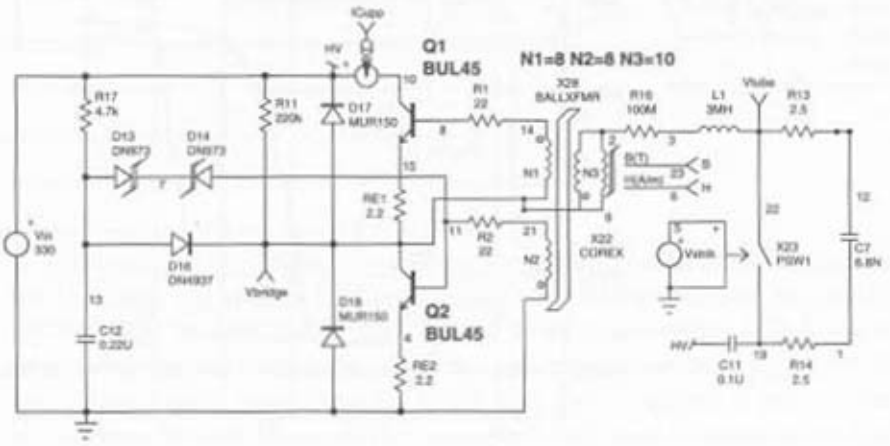


Figure 5-3a
An example of a bipolar, self-oscillating electronic ballast. Recent ON Semiconductor bipolar series even integrates the free-wheel diodes.

Figure 5-3b details the saturable transformer operation, while Figure 5-3c offers a view of typical signals.

MOSFET Version

"... and then came the MOSFETs ..." said the bipolar product engineer, sweeping away a tear rolling on his cheek! Easier to drive, more robust than bipolars, MOSFETs had a natural role to play in the bipolar ballast tragedy. Figure 5-4a depicts a MOSFET-driven ballast where the freewheel diodes are part of the devices. Zener diodes D8/D9 prevent any lethal gate-source voltages. Figure 5-4b presents other relevant signals for the self-driven converter.

A Relaxing FLASH Lamp

By associating a spark gap and a flash lamp, it becomes possible to build a pulsed light generator that operates by itself. A spark gap acts like a short when fired. At rest, the spark gap seems transparent to the surrounding element; it behaves like a high-impedance device, weakly capacitive. When

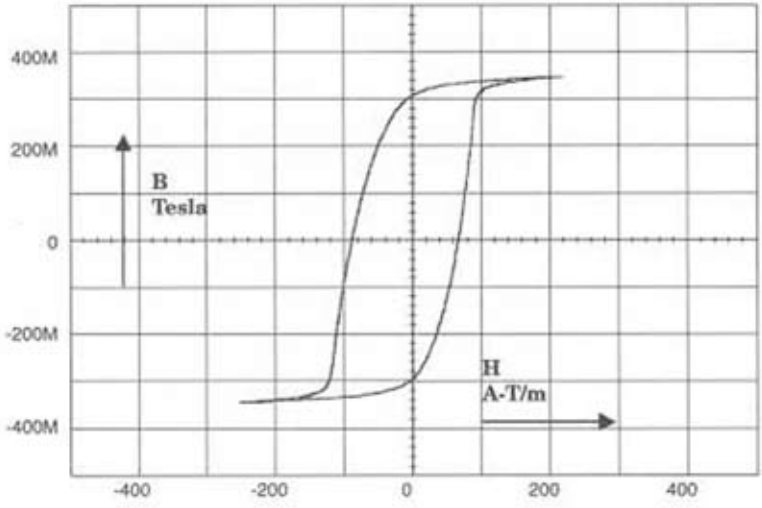


Figure 5-3b
The operating B-H curve at Plamp = 40W.

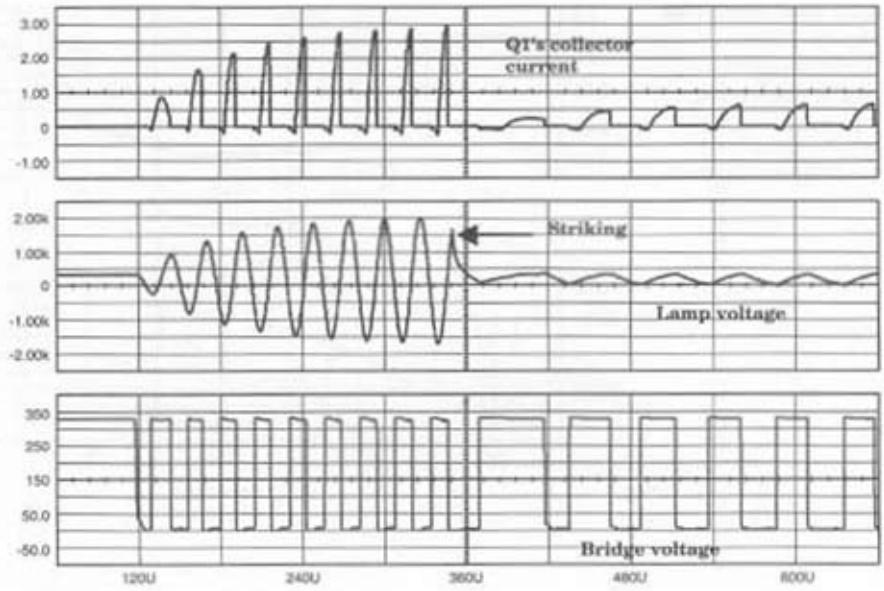


Figure 5-3c
Typical signals of the self-oscillating bipolar ballast

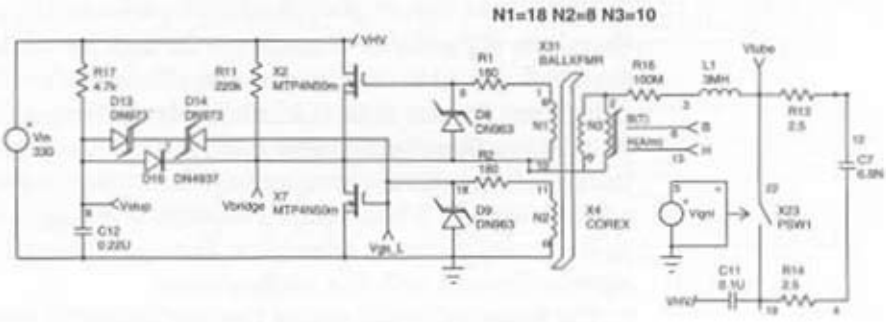


Figure 5-4a
MOSFETs require higher turn ratios than bipolar to properly drive them.

its terminal's voltage rises to the firing level, its internal gas gets ionized and the spark gap offers a low-impedance path. During this time, the spark-gap derivates most of the circuit current. When this current falls below a given level, the short disappears and the spark gap becomes a high-impedance dipole again. Describing the spark gap and its effects is beyond the scope of this chapter. However, the reader will find some information on two

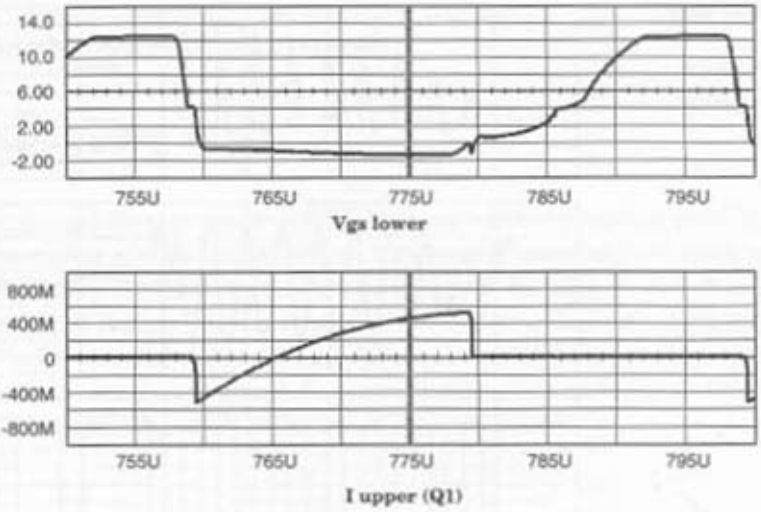


Figure 5-4b
The lower gate-source voltage with the upper MOSFET drain current.

dedicated Design Ideas published by the author in EDN and referenced by [33, 34]. The flash lamp operates roughly the same way except that you fire it through a dedicated pin.

Figure 5-5a depicts our pulsed light generator. At power-on, C3 starts to charge via R7, while C5 also charges through X9 winding and R13. Because the spark gap X1 is inactive, you also observe C3's voltage across its terminals. When X1 gets fired, it immediately discharges C5 within X9 primary. Thanks to a large transformer ratio, this voltage generates a large peak on the lamp firing pin; the lamp ionizes and C3 discharges through it. You have a flash! C3 and C5 being empty, X1 stops conducting, releasing C3's charge again. A new cycle can take place. Figure 5-5b portrays the low-frequency signals obtained with this configuration.

The following netlist details how the simplified flash lamp was built:

```
.subckt FLASH 1 2 3 {VTRIGG=8K VARC=150 ISUS=100M}
* A C Trigg
RDUM 3 0 100MEG
VDUM 1 10              ; Lamp current measurement
CPAR 1 2 1P            ; Open-lamp capacitance
RLEAK 1 2 10MEG        ; Open-Lamp leakage current
RNEG 10 11 -2          ; Negative behavior once struck
DTRK1 12 11 DCLAMP     ; Lamp voltage once struck, polar +
DSRK2 12 16 DCLAMP     ; Lamp voltage once struck, polar -
CARC 1 16 100pF        ; Arc capacitance
X1 16 2 13 SWITCH
```

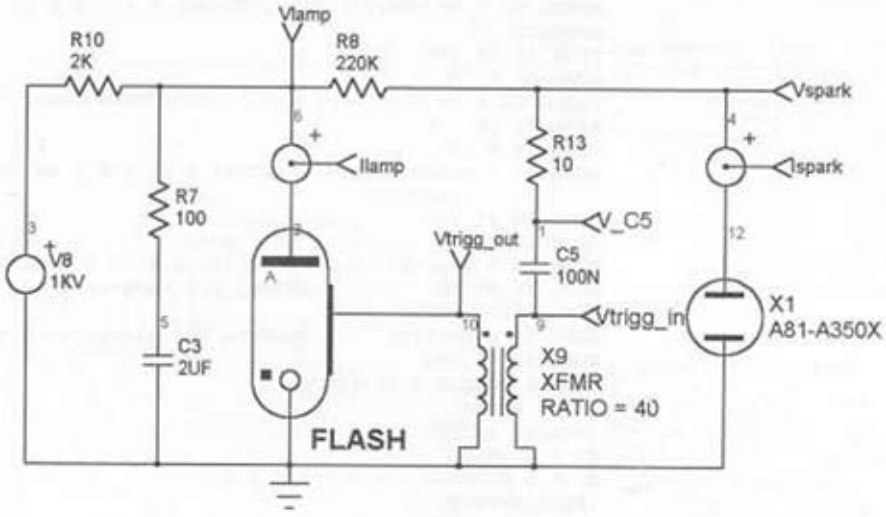


Figure 5-5a
A relaxing flash lamp using a sparkgap.

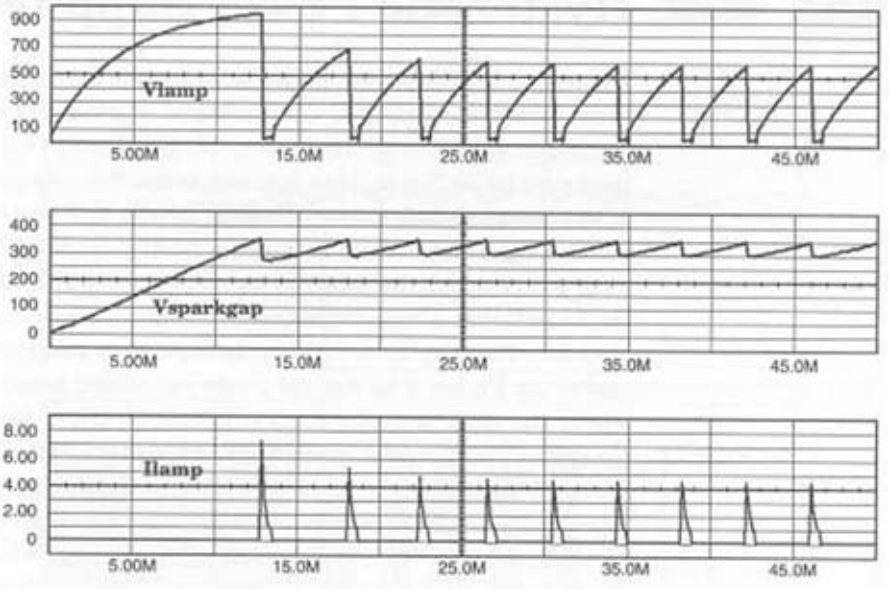


Figure 5-5b
Typical relaxing waveforms of the light flash.

```
BTRG1 41 0 V= ABS(V(2,3))>{VTRIGG} ? 1 : 0 ; Is applied field big
enough?
CTRG 41 50 10P
RTRG 50 0 1K
BTRG2 51 0 V= V(50)>0 ? 1 : 0 ; Electric field is pulsed
RPUL 51 46 100
CPUL 46 0 10P
BSUS 45 0 V=ABS(I(VDUM))>{ISUS} ? 1V : 0 ; Is ILAMP OK to keep lamp
        ;latched?
RSUS 45 47 100
CSUS 47 0 10P
BORS 15 0 V=(V(47)>0.5) | (V(46)>0.5) ? 100V : 0
RDEL 15 30 1K          ; Adjust the turn-on time
CDEL 30 0 100P
BDRV 31 0 V=V(30)      ; Buffers the signal to drive X1
RDRV 31 13 100
.MODEL DCLAMP D BV={VARC}
.ENDS FLASH
.SUBCKT SWITCH 1 2 3
R1 1 2 1E10
G1 1 2 POLY(2) 1 2 3 0 0 0 0 0 1
.ENDS SWITCH
```

Hysteretic Power Supplies

Hysteretic SMPS do not really fall into the self-oscillating section of this book. However, thanks to their natural dependence upon the circuit time constants, we believed they can be placed there. A hysteretic power supply uses a gated oscillator. That is to say, when the output voltage is below level 1, the power switch is permanently driven ON and OFF (the off event is usually based on a fixed maximum peak current) at the clock rate. When level 1 is reached, the internal logic stops the switch signal, and the output starts to fall at a rate dependent upon the Rload Cout combination. When Vout has dropped below level 2, the logic then reactivates the power switch and so on. Figure 5-6a depicts a very simplified gated FLYBACK converter where the clock sets the latch every cycle. When the current reaches the maximum peak value given by Rsense (1V/6.8Ω), the switch opens and stays off until the next clock cycle. Since Vout is below level 1, CMP stays high and authorizes pulses to go through the AND gate. When level 1 is finally reached, CMP goes low and prevents any switching operation; Vout starts to fall until level 2 is reached. CMP goes high, and the switch can be driven again. The resulting Vout is made of a ripple (level 1 − level 2) of amplitude and centered at an average value of (level 1 + level 2) / 2. (See Figure 5-6b.)

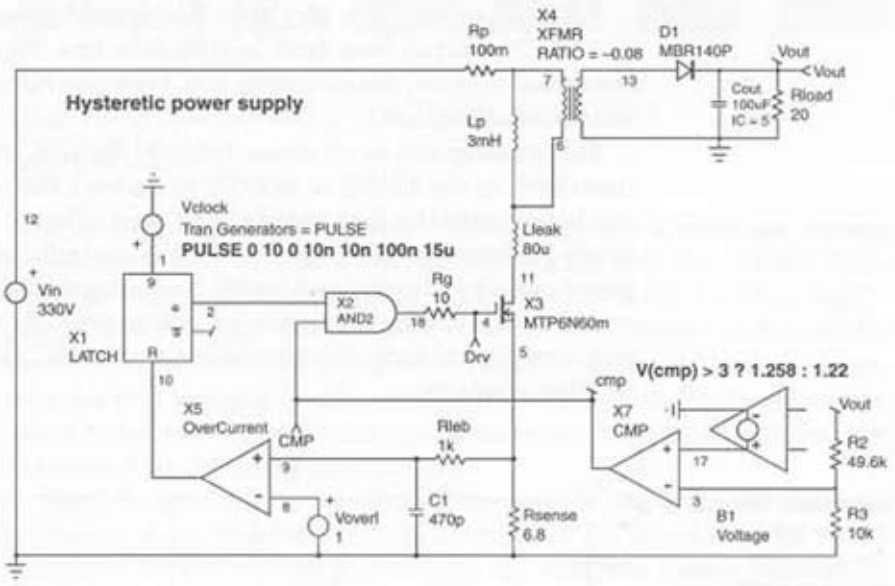


Figure 5-6a
A simplified hysteretic FLYBACK converter regulating around 7V.

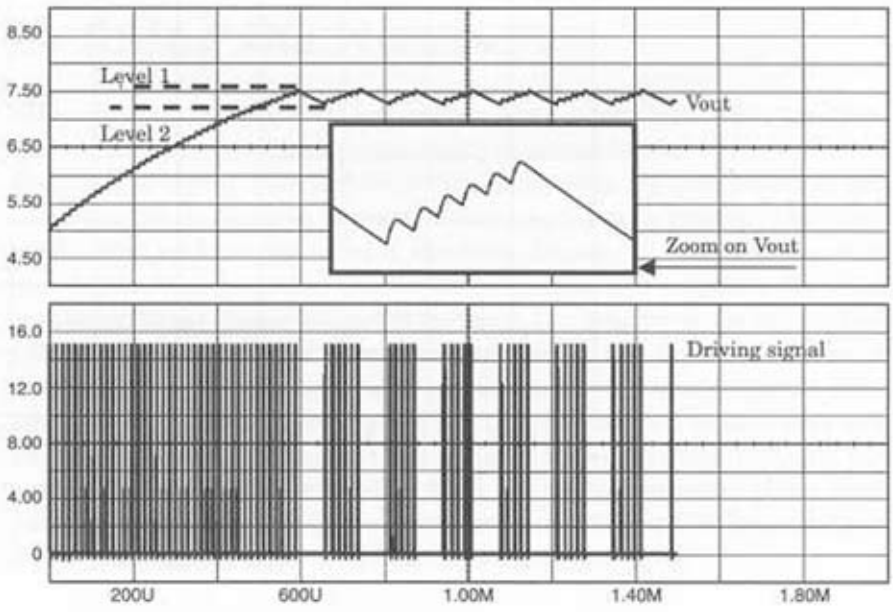


Figure 5-6b
Start-up sequence followed by the steady-state operation.

A hysteretic SMPS is very fast. To test this statement, we excited the FLYBACK's output from 5mA to 400mA in 1ms. Figure 5-6c portrays the result and confirms the extremely small reaction time of the converter with nearly no undershoot.

This topology can be implemented in FLYBACK, but also in other structures such as the BUCK or BOOST. At no-load, the switch driving frames can be separated by long periods of off time, offering an excellent standby power performance. However, due to its uncontrolled nature, the hysteretic power supply is rarely used in RF applications. Also, the covering of the audible range while working can sometimes present some drawbacks to the end-user. Typical hysteretic controllers are the MC34063 or MC34163 from ON Semiconductor.

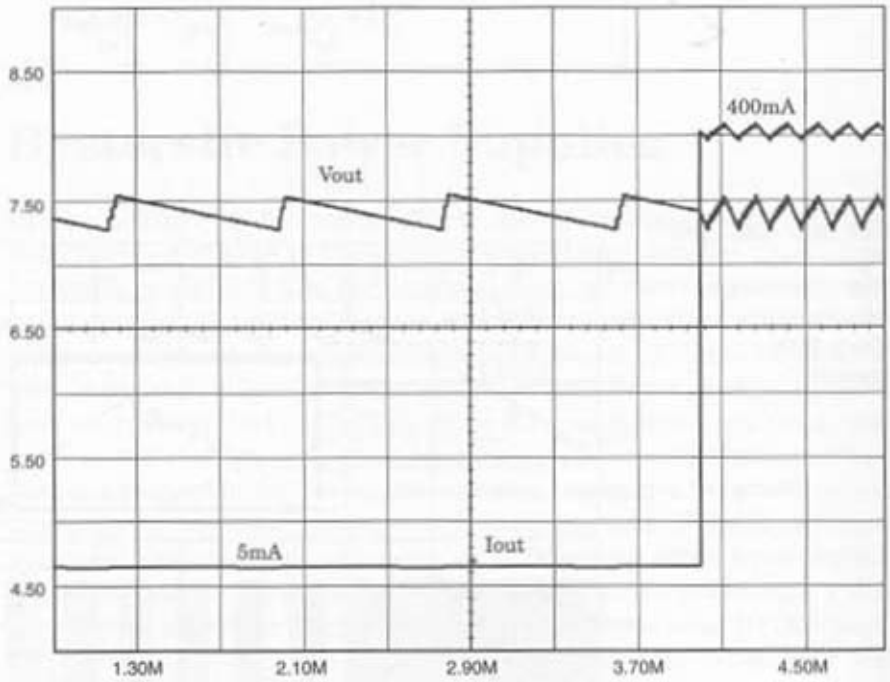


Figure 5-6c
The load step response of the hysteretic power supply is extremely short.

APPENDIX A

Applying the K Factor for Quick Pole-Zero Compensation

Analyzing and compensating the feedback loop of a system has always been thought of as an expert exercise. Fortunately, with the help of a dedicated tool like the K factor, loop compensation really becomes child's play . . . on the paper! This last statement simply means that once the method has delivered the poles/zeroes location, you must absolutely measure the true physical results with a network analyzer. Further iteration might be necessary to refine the results and reach the wanted performance in terms of bandwidth or response time.

The K factor was introduced by a pioneer of the SMPS bandwidth measurements, Dean Venable. Without entering into the details through which he defined the tool, we will go directly to the equations needed to calculate the element values. As usual, we encourage you to read his paper as referenced by [29].

Defining the Numbers

When you want to close the loop with a given bandwidth (BW), you have derived the location of the compensating elements further to the open-loop Bode plot analysis. The first step thus deals with the generation of this amplitude/phase diagram. It now becomes an easy task, thanks to the averaged model we have described in the book (Figure A-1). Once you have it, you decide the necessary bandwidth you need and calculate the final amplitude/phase implications: For instance, you might want to cut the loop gain at 10kHz (where the closed-loop gain will in fact cross the 0dB axis). On Figure A-1, you extract a value of −23dB. You will thus tailor the error amplifier response to deliver +23dB at 10kHz and then further decrease the response to secure the gain margin (gm). From the phase plot, you will see how far you are from the −180° limit and see the necessary phase boost you will need to be perfectly stable at the desired 10kHz BW. Depending on these gain/phase numbers, you select the amplifier types.

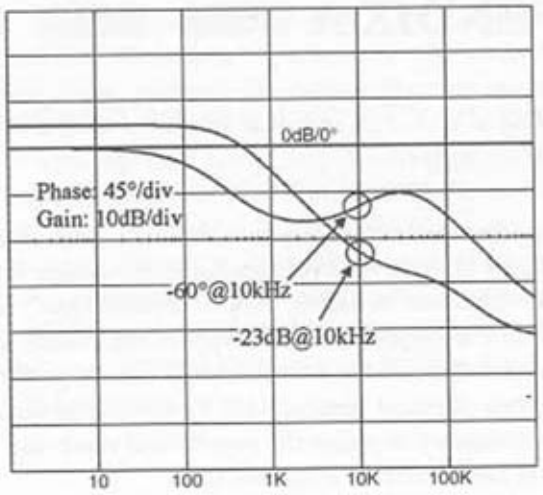


Figure A-1
A typical open-loop Bode plot for a DCM BOOST converter

Amplifier Types

Dean Venable defined three different types of error amplifiers depending on the phase boost you finally want:

Type 1: This amplifier is nothing else than an integrator as depicted by Figure A-2. It will not provide any phase boost and it is usually selected when you want to roll-off the gain before the peaking of an LC filter appears.

The DC gain of the system is defined by: $\frac{Rlower}{Rlower + Ruper} \cdot A_{OL}$ where A_{OL} represents the open-loop gain of the operational amplifier. The NINV pin is normally connected to the reference. Please note that we do not have a DC virtual ground on the schematic because the OPAMP lacks a DC feedback: Rlower thus plays a role in the DC gain. However, because the OPAMP actually closes its loop in AC, a virtual ground appears and the circuit fights to equilibrate both inputs to zero. In that case, Rlower is no longer active and Rupper alone introduces the pole at:

$$Fp = \frac{1}{2 \cdot \pi \cdot Rupper \cdot C1}.$$

Type 2: The type 2 amplifier is one of the most common implementations found in SMPS designs, as Figure A-3 details. This struc-

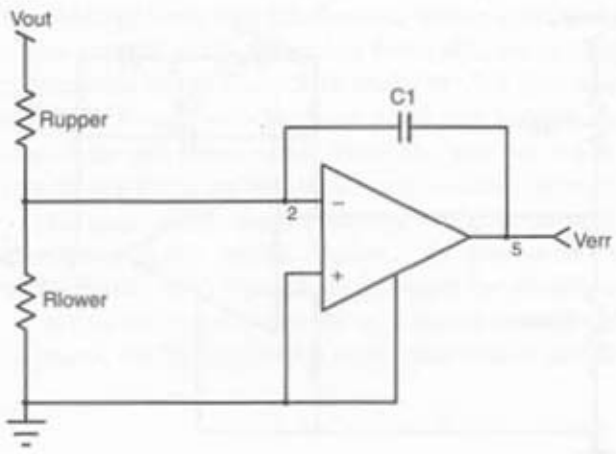


Figure A-2
A type 1 amplifier features a pole at the origin.

ture is well-suited for the majority of DCM supplies exhibiting a first-order behavior. It actually creates a flat gain region preceded and followed by two −20dB/decade slopes (also called −1 slope). In this flat region, the circuit offers a phase boost up to 90°. In practice, you will select the type 2 amplifier when less than 70° phase boost is required.

This configuration introduces the following poles/zeroes:

$Fp = \frac{1}{2 \cdot \pi \cdot R2 \cdot C2}$ $Fz = \frac{1}{2 \cdot \pi \cdot R2 \cdot C1}$. Again, Rlower does not play a role in the AC gain, but surely does in the DC portion.

Type 3: The type 3 amplifier becomes interesting in converters where you need a large phase boost, up to 180°. The situation typically occurs in CCM converters. Figure A-4 shows this latest structure:

This configuration introduces the following poles/zeroes:

$Fp1 = \frac{1}{2 \cdot \pi \cdot R2 \cdot C2}$ $Fp2 = \frac{1}{2 \cdot \pi \cdot R3 \cdot C3}$ $Fz1 = \frac{1}{2 \cdot \pi \cdot R2 \cdot C1}$

$Fz2 = \frac{1}{2 \cdot \pi \cdot Rupper \cdot C3}$. Again, Rlower does not play a role in the AC gain, but surely does in the DC portion.

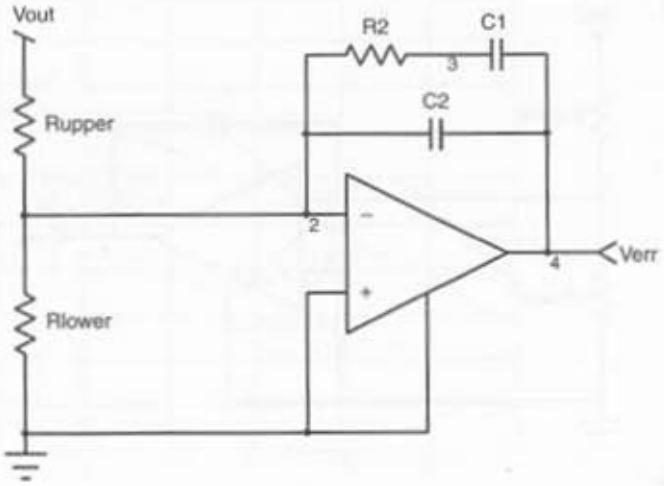


Figure A-3
A type 2 amplifier as depicted by Venable.

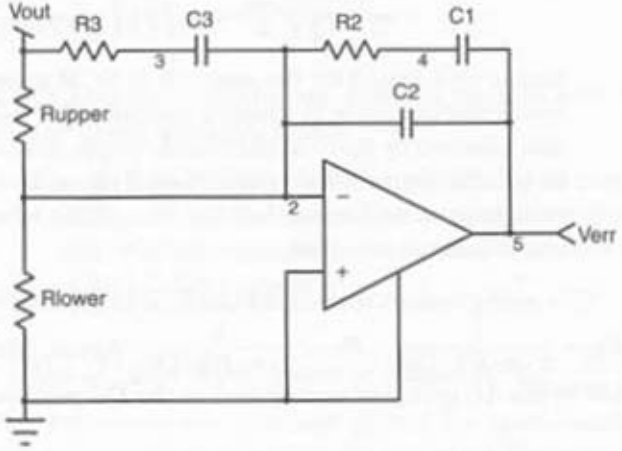


Figure A-4
A type 3 amplifier provides up to 180° phase boost.

Closing the Loop

Let's stick to the Figure A-1 Bode plot and try to reach our 10kHz bandwidth. Because we are not really bothered by the phase margin, we will select a type 2 amplifier. We compiled the Venable calculation steps in an Excel spreadsheet called *k factor.xls*, which is available on the CD-ROM. By entering the values directly taken from the open-loop Bode plot, the

spreadsheet computes the element values to reach our goals: BW = 10kHz, phase margin = 45°. From the Bode plot, we extract the amplitude/phase parameters at 10kHz: −23dB and −60°. We thus need to shift up the curve by 23dB. Please note that we could also enter a negative number if the open-loop gain was higher than the one we really need. The computed results are given on Figure A-5, which hard-copies the Excel screen.

The simulation example uses a BOOST operating in DCM and implementing Ridley's model. Figure A-6a depicts the application schematic while Figure A-6b unveils the obtained bandwidth (on the Verr probe).

As you can see, the results correspond exactly with what we were looking for: a 10kHz bandwidth associated with a 45° phase margin.

Figure A-5
Excel computes the passive element values for you.

Type 2 Amplifier. Required boost less than 90° (less than 70°, in practice)

Design parameters	
Cross-over frequency Fc (Hz):	10000
Phase margin (degrees):	45
Upper feedback resistor (ohms):	10000
Parameters extracted from Bode plot	
Gain to reach 0dB at Fc (pos. or neg. dBs):	23
Phase at Fc (**negative** degrees):	-60
Calculated parameters	
Phase Boost	15
K	1.303225373
C2 (pF)	86.45708822
C1 (nF)	0.060381317
R2 (kohms)	343.5081762
1st Pole, C2-R2	5358.983849
1st Zero, C1-R2	7673.26988

You put positive gain if you need to push up the gain curve

You put negative gain if you need to pull down the gain curve

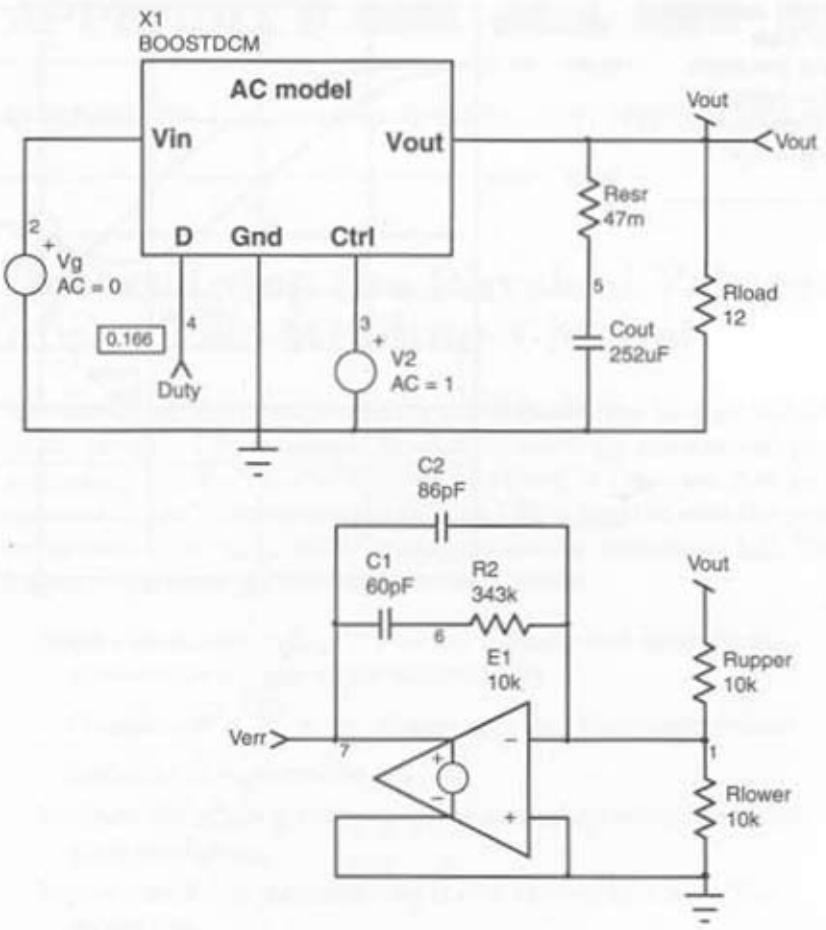


Figure A-6a
The DCM BOOST we have tailored to a 10kHz bandwidth.

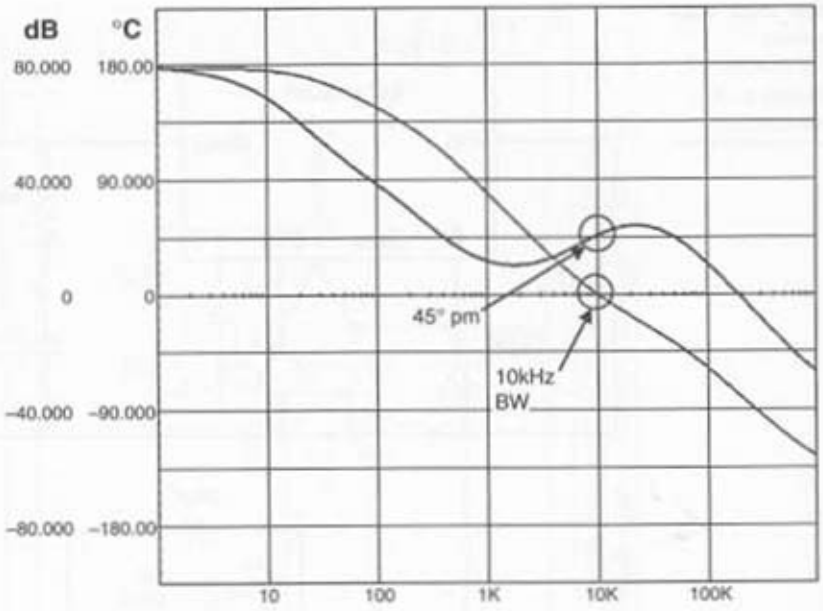


Figure A-6b
The final simulation results showing a good agreement with the design goals.

APPENDIX B

Feeding the Transformer Models with Physical Values

Determining the Physical Values of the Two-Winding T-Model

You often read: Short the secondary and measure the leakage inductance on the primary. This statement depends on the model you have adopted for simulation. For the T model depicted by Figure B-1, you see that you will measure the reflected secondary leakage L*l*2 in parallel with the primary inductance, all in series with the primary leakage inductance L*l*1. The following steps detail the procedure for the T model:

Inject a sinusoidal voltage Vp on the primary and measure the open-circuit voltage on the secondary Vs.

Compute $N = \frac{Np}{Ns} = \frac{Vp}{Vs}$. Please note that this measurement neglects Ll1 compared to Lm.

Measure the primary inductance, the secondary being open. This gives you Lps_{open}.

Repeat step 2, but the secondary is now shorted by a wire. You obtain Lps_{short}.

Compute the coupling coefficient k with: $k = \sqrt{1 - \frac{Lps_{short}}{Lps_{open}}}$.

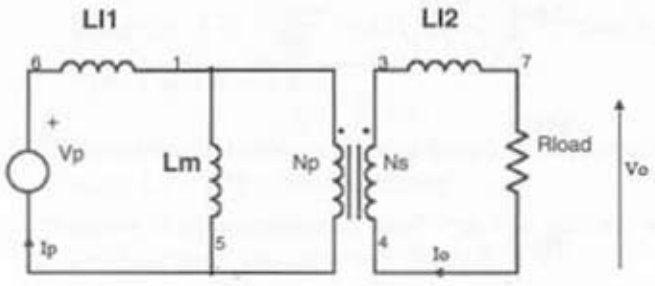


Figure B-1
The T model used in our transformer SPICE model.

Compute Ll1 with: $Ll1 = (1 - k) \cdot Lps_{open}$

Compute Ll2 with: $Ll2 = (1 - k) \cdot Lps_{open} \cdot \frac{1}{N^2}$

Compute Lm with: $Lm = k \cdot Lps_{open}$

Measure with an ohm-meter the primary and secondary DC resistances, respectively Rp and Rs, and bring those values to the transformer netlist as Figure B-2 portrays.

The Three-Winding T-Model

The final three-winding model appears in Figure B-3, where three leakage elements appear in series with each winding. The surprise comes from the primary leakage element, which depends upon the primary leakage air path P1 but also from the permeance P23 between both secondary windings. As a matter of fact, if you improve the coupling between both secondaries (for example, by twisting the wires), you *increase* the primary leakage inductance. Reference [32] paper also demonstrated how the leakage elements stay practically independent of the air-gap length: The coupling coefficient diminishes as the air-gap increases (the magnetizing inductance becomes smaller), but leakage elements stay constant.

Leakage elements definitions:

$Ll1 \approx n_1^2 \cdot (P1 + P23)$ Primary Winding

$Ll2 \approx n_2^2 \cdot (P2 + P13)$ Power Winding

$Ll3 \approx n_3^2 \cdot (P3 + P12)$ Auxiliary Winding

$Mo \approx n_1^2 \cdot (Pm)$

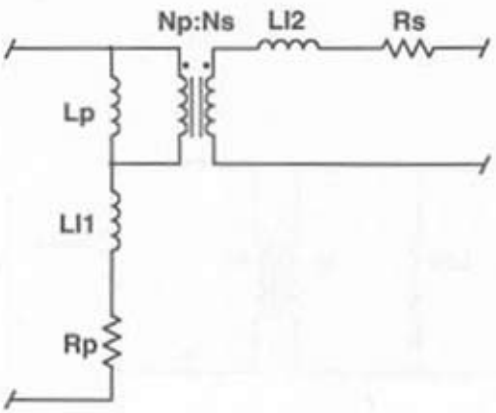


Figure B-2
The complete two-winding transformer SPICE model.

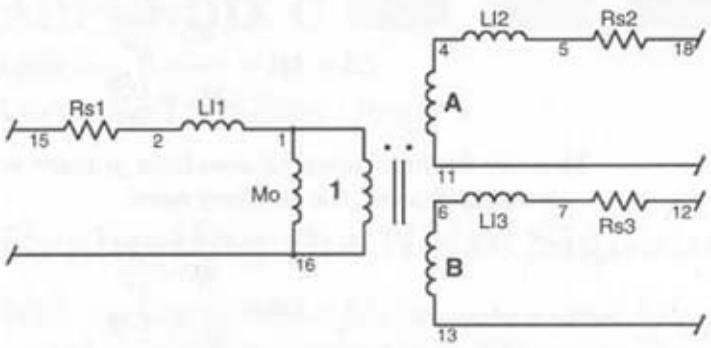


Figure B-3
Final equivalent model showing every leakage elements.

Determining the Physical Values of the Three-Winding Model

These measurements require an RLC bridge or a network analyzer operating at a frequency high enough to neglect the winding resistance (if you measure an impedance), but low enough to minimize the interwinding capacitances. In our numerical application, we selected 100kHz, which is the operating frequency of our converter. The network analyzer gives you a complete impedance-phase plot, and ensures that you stay on the inductive portion during the measurement. With a standard LRC-meter, if changes in the operating frequency do not lead to big variations in the values you read, then you are well on the inductive portion.

The following steps express how you combine the various leakage elements from the measurement data and feed the SPICE model with the results (numbers are examples coming from a real transformer):

Inject a sinusoidal voltage Vp on the primary and measure the open-circuit voltages on the secondaries Vs_{power} and $Vs_{auxiliary}$. Compute $A = \frac{Vs_{power}}{Vp}$ and $B = \frac{Vs_{auxiliary}}{Vp}$. Measures gave A = 0.0817 and B = 0.156.

Measure the inductance L1 seen from the primary, the secondaries open: $L1 = Ll1 + Mo = 3.62mH$.

Measure the inductance L2 seen from the primary with the power winding open, the auxiliary shorted:

$$L2 = Ll1 + \frac{Mo \cdot \frac{Ll3}{B^2}}{Mo + \frac{Ll3}{B^2}} = 199\mu H$$

Measure the inductance L3 seen from primary with the power winding shorted, the auxiliary open:

$$L3 = Ll1 + \frac{Mo \cdot \frac{Ll2}{A^2}}{Mo + \frac{Ll2}{A^2}} = 127\mu H$$

Measure the inductance L4 seen from the power winding, the auxiliary shorted and the primary open:

$$L4 = Ll2 + A^2 \cdot \left[\frac{Mo \cdot \frac{Ll3}{B^2}}{M0 + \frac{Ll3}{B^2}} \right] = 1.405\mu H$$

Please note that L1-L4 could also be impedances Z1-Z4. You should then divide each value by $2.\pi.F_{measure}$ to obtain the inductance value. We now have a system of four equations with four unknowns. Feeding a math processor with these equations give the solutions in a snapshot:

$$Ll1 = \sqrt{\left(L3 - L1 - \frac{L4}{A^2}\right)(L3 - L1)} + L1 = 58.85\mu H$$

$$Ll2 = \frac{A^2 \cdot (Ll1 - L1) \cdot (L3 - Ll1)}{L3 - L1} = 466nH$$

$$Ll3 = \frac{B^2 \cdot (Ll1 - L1) \cdot (L2 - Ll1)}{L2 - L1} = 3.558\mu H$$

$$Mo = L1 - Ll1 = 3.56mH$$

Series resistances are measured with a 4-wire ohm meter and included in the SPICE model.

APPENDIX C

Conducted EMI Filter Design

Evaluating the Noise Signature

In this appendix, we will compare the results obtained from simulation versus real measurements delivered by an EMI receiver. Figure C-1a depicts our simulation template, following the guidelines described in Chapter 4. You see a typical SMPS circuit built around the NCP1200 from ON Semiconductor, a device specifically introduced to let you design power supplies in a very short time:

- **No need of auxiliary winding:** The technology lets you supply the IC directly from the high-voltage DC rail. This is called *Dynamic Self-Supply* (DSS). In battery charger applications, you no longer need to design a special primary circuitry to cope with the transient lack of auxiliary voltage (for example, Vout is low).
- **Short-circuit protection:** By permanently monitoring the feedback line activity, the IC is able to detect the presence of a short circuit, immediately reducing the output power for a total system protection. Once the short has disappeared, the controller resumes and goes back to normal operation. For given applications (for example, constant output power supplies), you can easily disconnect this protective feature.
- **Low standby-power:** If SMPSs naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP1200 drastically reduces the power wasted during light load conditions. In no-load conditions, the NPC1200 enables the total standby power to easily reach the next International Energy Agency (IEA) recommendations.
- **No acoustic noise while operating:** Instead of skipping cycles at high-peak currents, the NCP1200 waits until the peak current demand falls below a user-adjustable one-third of the maximum limit. As a result, cycle skipping can take place without having a singing transformer. You can thus select cheap magnetic components free of noise problems.

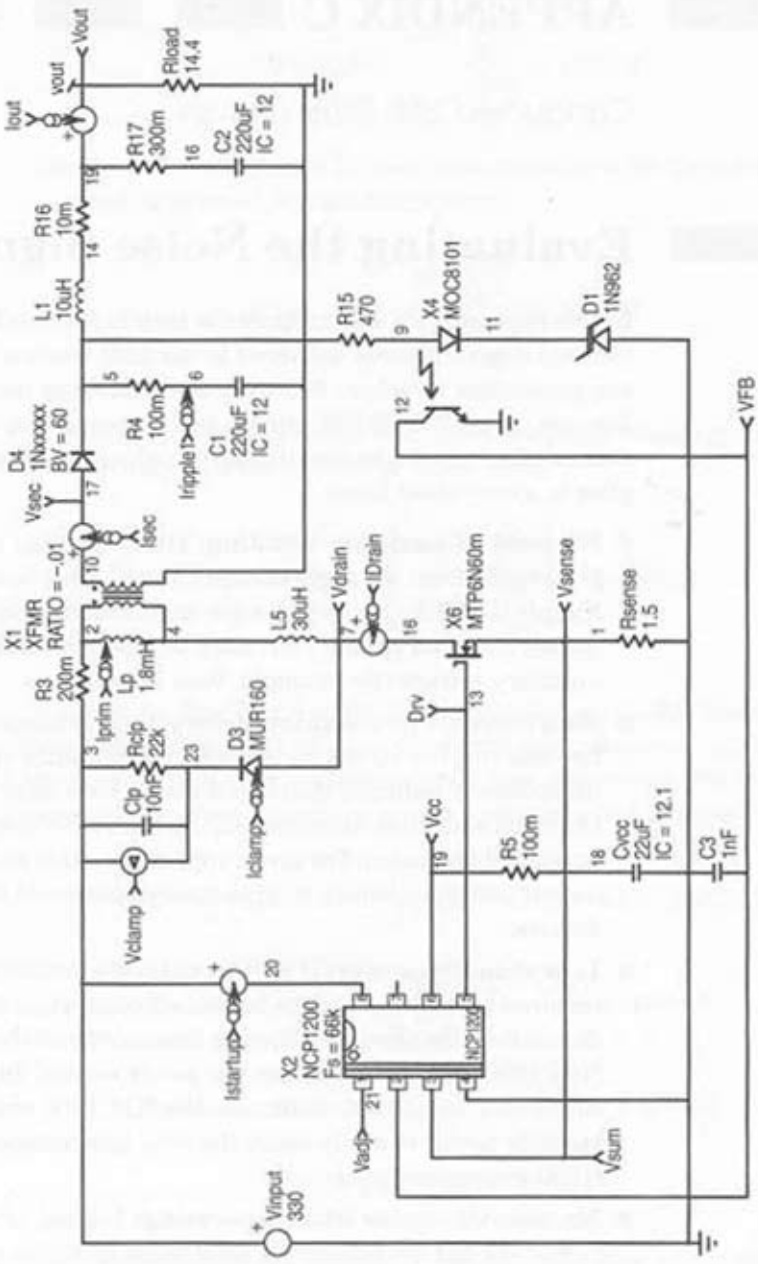


Figure C-1a
A complete offline simulation template to unveil the desired operating point.

Instead of routing the noise signal through a simplified LISN network, we have reproduced a true device whose netlist is given at the end of this appendix. It appears in Figure C-1b where the equivalent bulk capacitor model has been installed.

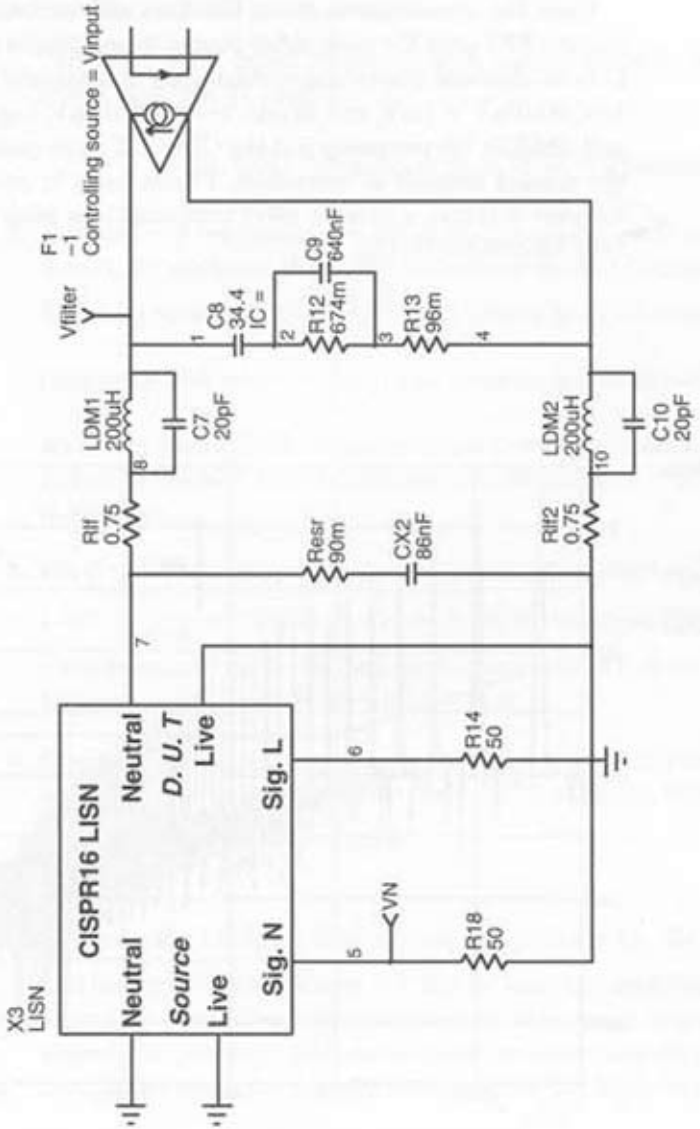


Figure C-1b
. . . while the input EMI fixture lets you analyze the SMPS signature.

This application represents a 10W universal input AC/DC wall adapter operating during given load/line conditions. To unmask the harmonics, F1 current-controlled current source routes the high-frequency current pulses through the equivalent model of our 33µF capacitor and develops the unwanted noise signal. This signal is confronted to the 50Ω LISN network and a final reading is made on one of the outputs. For simulation reasons, we only use one input, the other one being loaded by a 50Ω resistor.

Once the simulation is done, the data manipulation interface lets you run the FFT over VN node. After proper formatting, a graph such as Figure C-1c is obtained where the vertical axis is displayed in dBµV (0 dBµV = 1µV, 60dBµV = 1mV, and so on). To obtain dBµV, Log compress the Y axis and add 120. We purposely put the CISPR22 class quasipeak limit to assess the needed amount of correction. Please keep in mind that a quasipeak detector will give a smaller level compared to a peak detector as we naturally have with SPICE.

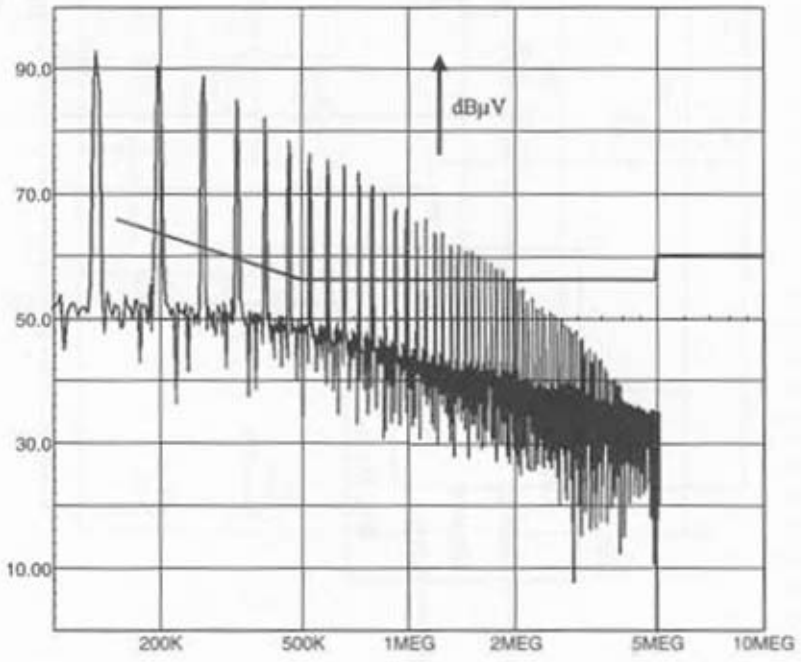


Figure C-1c
Further to the simulation, an FFT plot is drawn by the graphical interface.

Calculating the Required Attenuation

From this graph, we can clearly identify the value of the highest harmonic: 90 dBμV @ 190kHz (below 150kHz is out of the CISPR22 sweep range). To pass the limit, we shall reduce its contribution by more than 35 dB, taking into account a 10dB safety margin:

1. Position the LC cutoff frequency fc at a given value to obtain the above rejection at 190kHz:

$$-35 = -40 \cdot \mathrm{LOG}(190k/fc) \text{ or } fc = \frac{190k}{10^{\frac{35}{40}}} = 25.3\mathrm{kHz}.$$

2. To avoid any resonance, the filter quality coefficient Q should be less than 1. By applying the Q definition for a series LC filter, we obtain the following equation: $Q = \frac{\omega o \cdot L}{Rs} < 1$ where Rs is the total series resistance and $\omega o = \frac{1}{\sqrt{L \cdot C}}$. The resistance Rs will normally include all ohmic losses (ESR, inductor series resistance, load, and so forth), but since the 50Ω load dominates, we will make Rs = 50 for our calculation.

3. Fix C to an arbitrary 100nF value (for the first step) and calculate L by: $\frac{Rs}{2 \cdot \pi \cdot fc} = 315\mu\mathrm{H}$. L should be in the range of 200–400μH if you want to benefit from CM leakage inductances. If L is too big, select a bigger capacitor 220nF, 330nF, or 470nF.

4. Check the DC input impedance presented by the SMPS at the lowest line condition (η = 75%): Pin = Pout / 0.75 = 13.3W. With a 120VDC input, Rin $= \frac{VinDC^2}{P} = 1082\Omega$.

5. Evaluate the LC filter characteristic impedance by: $Zo = \sqrt{\frac{L}{C}} = 56\Omega$ and be sure to follow Zmax << Rin to keep the stability. A plot example of the filter output impedance will reveal Zmax (the output impedance peaking) and ensure that the above stability criterion is met. It can easily be done by sweeping the LC filter output terminal

through a 1A AC source. Observing the terminal voltage will display ohms. In our application, the peaking shows a value of

$$Zmax = \frac{Zo^2}{Rs} \cdot \sqrt{1 + \left(\frac{Rs}{Zo}\right)^2}$$ or 38.5dBΩ with our application values.

(See Figure C-2a.)

The exercise can be completed by sweeping the input impedance of the supply through its average model and pasting the results on Fig. C1.2b graph: there should be no overlap between the plots.

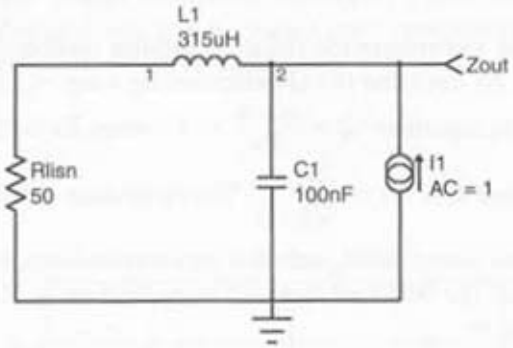


Figure C-2a
By fixing the AC current source to 1A, the voltage probe Zout directly gives ohms.

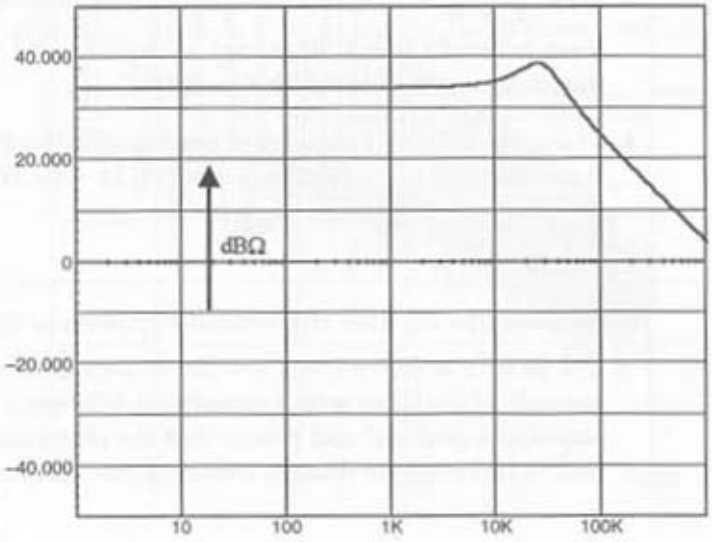


Figure C-2b
This voltage plot shows an output impedance affected by a low peaking.

The Final Filter Stage

We now have the choice to combine a CM filter together with a single inductor for the DM currents. Another option is to select a CM filter inductance knowing its leakage inductance and take benefit from it for a DM cure. For a DM inductance below 500µH, a 27mH CM inductor can be a good choice. However, we need to precisely evaluate the available leakage inductance. With a 1:1 ratio, differential currents cancel the internal field. As a result, why not connect the dotted ends of the choke and naturally circulate differential currents while measuring the inductance. This is what is proposed by Figure C-3a.

Figure C-3b finally gives you the final impedance plot of the leakage inductor, showing various stages: resistive in the lower portion, inductive in the medium portion, and finally capacitive for higher frequencies. At 100kHz, we can read 48dBΩ or a 250Ω impedance. The final calculation leads to an inductance of 398µH or twice 199µH when split into two components. Figure C-3c gives its equivalent SPICE model with ohmic losses measured with a 4-wire multimeter.

Following are measurement results comparing CM inductors provided by two different manufacturers:

Schaffner RN1140-08/2: Lopen = 23mH, Lleak = 238µH or $2 \times 119\mu H$.

Siemens B82723A2102-N1 Lopen = 31mH, Lleak = 398µH or $2 \times 200\mu H$.

As you can imagine, combining the 100nF-X2 capacitor (who also has parasitic elements) together with a Figure C-3c-like inductor will deliver a result different from what we expect. Actually, the best would be to assess the final attenuation from the input of the filter (where the diode bridge connects) to the final output of the EMI receiver. SPICE does it in a snapshot as shown by Figures C-3d and 3e.

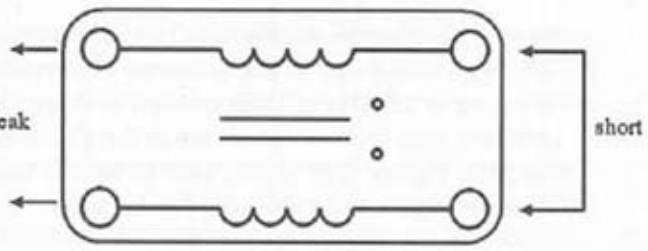


Figure C-3a
Shorting the dot-ended windings gives you the value of the total leakage inductance.

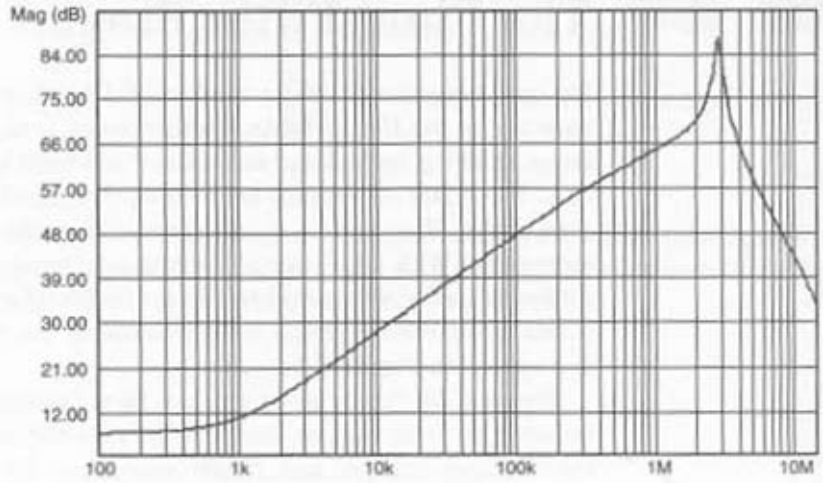


Figure C-3b
A leakage inductance also welcomes parasitic elements.

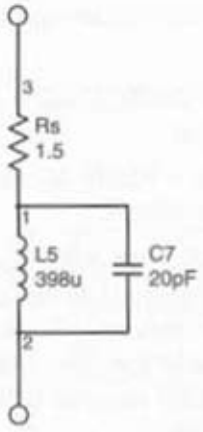


Figure C-3c
These elements can be modeled using SPICE.

As you can observe on Figure C-3e, the rejection tends to degrade at higher frequencies due to the presence of parasitic components. But our attenuation at 190kHz is 33dB, enough to theoretically pass the DM test.

Let's now plug all these elements in the Figure C-1b test fixture and run a new test. Figure C-3f shows how to install these elements before the LISN while Figure C-3g plots the final results.

On the paper, we pass the test for DM measurements.

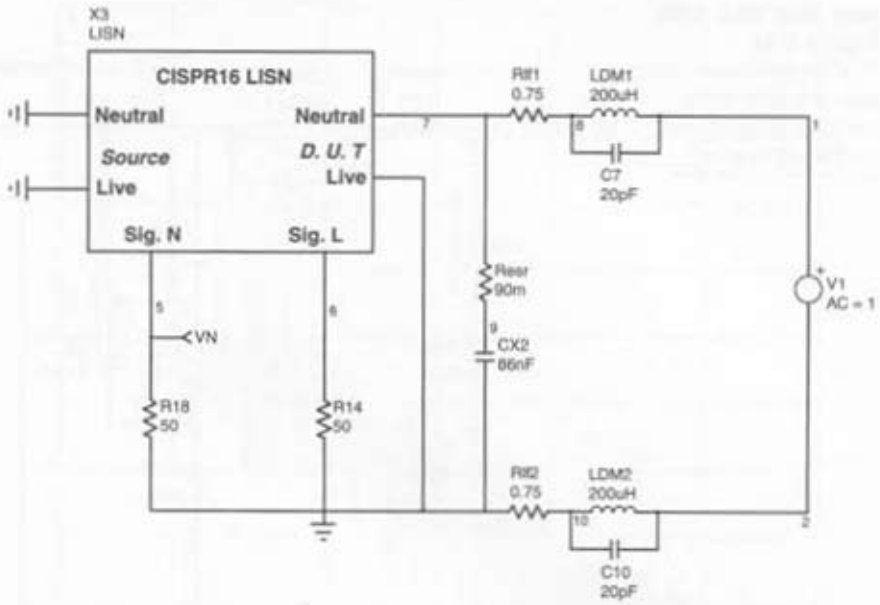


Figure C-3d
This sketch lets you evaluate the filter attenuation once loaded by the LISN device.

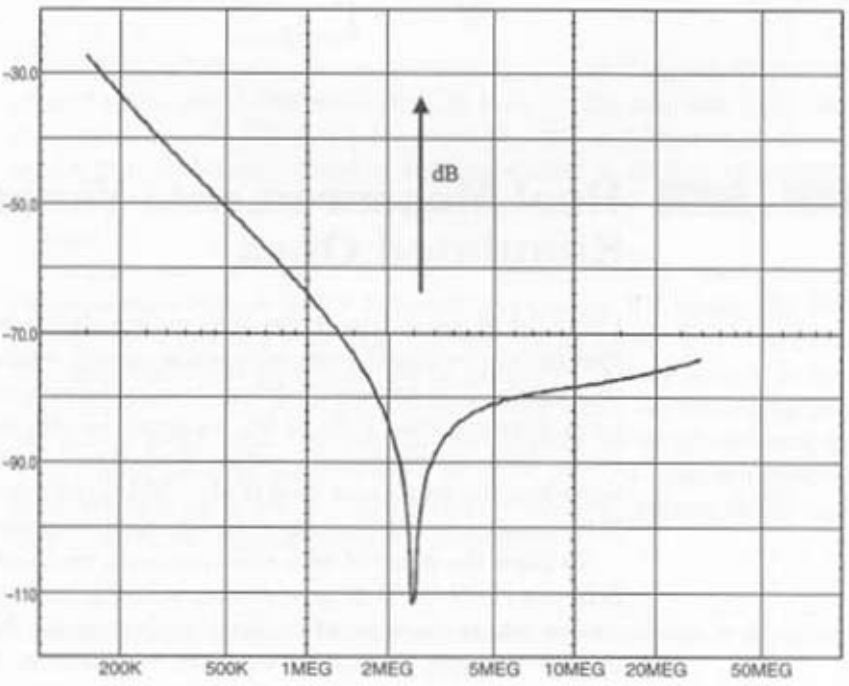


Figure C-3e
The resulting final attenuation versus frequency.

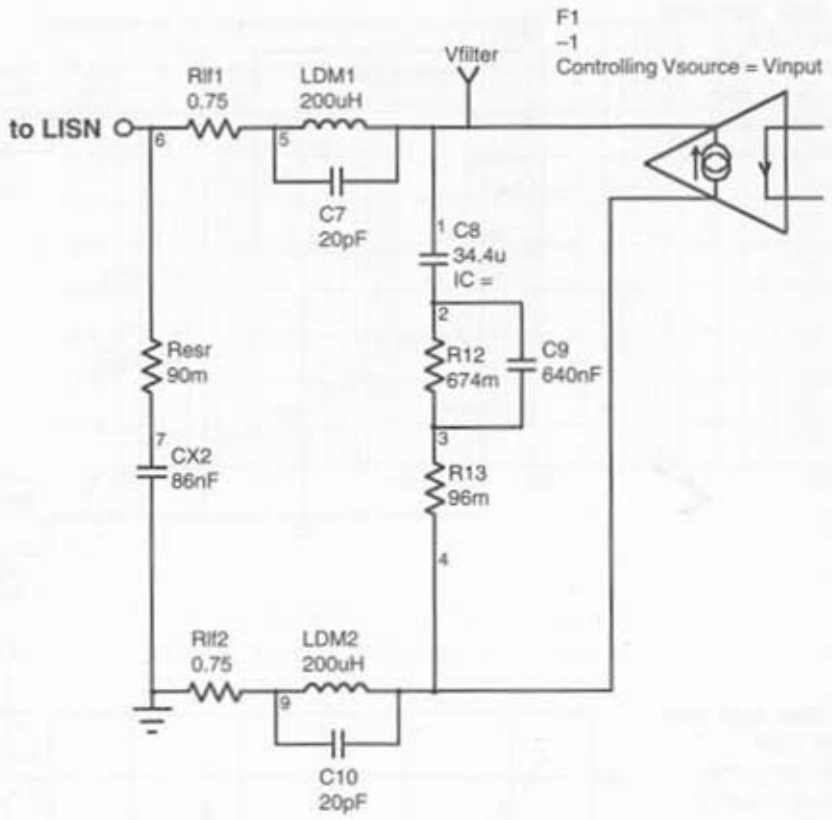


Figure C-3f
This sketch shows how the filter finally behaves once loaded by the LISN device.

Real Measurements Versus Simulated Ones

Using the aforementioned approach, we are able to design a filter in a few iterations providing the computer is fast enough when running SPICE. But this approach is not worthwhile if true measurements on a board reveal large discrepancies. First of all, we must be able to extract differential mode from common-mode noise. Unfortunately, standards fix limits regarding the total noise level (CM + DM) available on either L1 (live) or N (neutral), a switch routing either line to the receiver.

To allow the study of both noise contents, we have modified a Rhode & Schwarz LISN (ESH-3) to which we added a second separated output. A switch simply loads one of the lines while running the final measurement on the other one. We now have L1 and N separated. If DM currents circu-

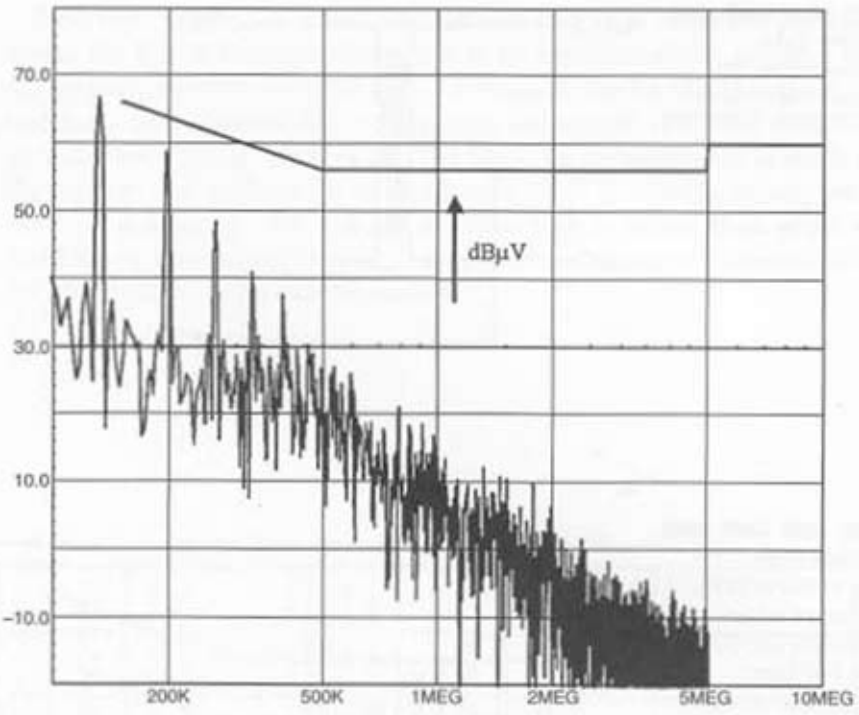


Figure C-3g
The resulting spectrum confirming the filter action.

late 180° out of phase on the lines, summing L1 and N signals theoretically gives 0 while you obtain twice the CM level. At the opposite, subtracting the signals cancels CM and gives twice the DM. One limitation, however, exists: The impedance offered by both lines shall be perfectly equilibrated over the frequency range of interest; otherwise the rejection ratio will change.

We have used an AEMC (Seyssins, France)[1] DM/CM extractor to perform our tests (Figure C-4a). Figure C-4b plots the DM quasipeak SMPS signature without any EMI filter obtained with a Rhode & Schwarz ESPC EMI receiver. These results should be compared to the Figure C-1c drawing. The error on the main peak is only 8dBs, while the remaining peaks are not far away. Also, quasipeak measurements deliver levels lower than with a peak detector. Keep in mind that the DM/CM extractor ensures a good rejection up to 1MHz (60dB), while it tends to degrade in the higher portion. Still, the overall result is encouraging.

1. AEMC, 86 rue de la Liberté 31180 SEYSSINS France. Tel. 33 (0)4 76 49 76 76, Fax. 33 (0)4 76 21 23 9

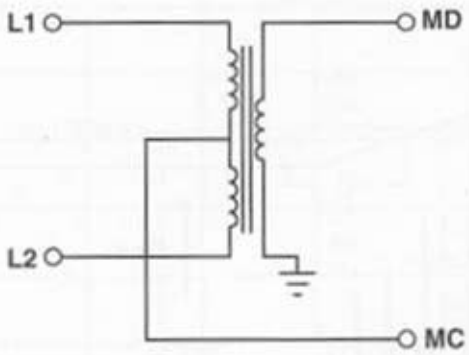


Figure C-4a
A transformer to extract DM from CM.

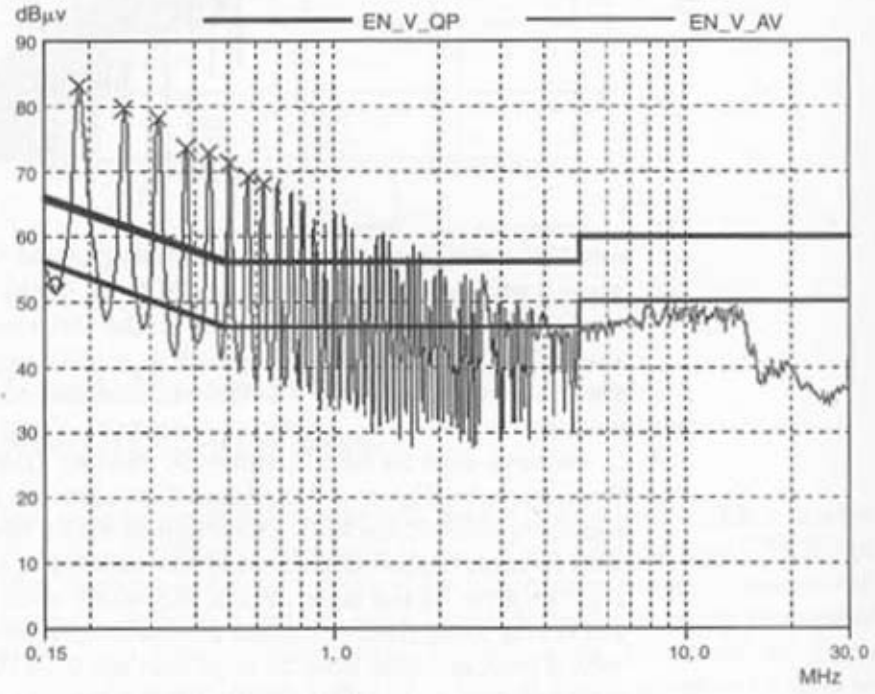


Figure C-4b
The DM-only SMPS signature when operated without any EMI filter (quasipeak detector).

Let's now connect our 27mH CM inductance with a 100nF-X2 capacitor across the line. If this capacitor needs to be increased above 100nF, a discharge path has to be provided to avoid electrical shocks when touching the terminals immediately after unplugging the supply (IEC-950 defines a time constant less or equal to 1s). The final DM measurement is given by Figure C-4c and confirms an attenuation of 35dB at 190kHz, exactly what we were looking for. The margin we have here is better than what we obtained in simulation, probably because of the quasipeak internal time constants used during measurements.

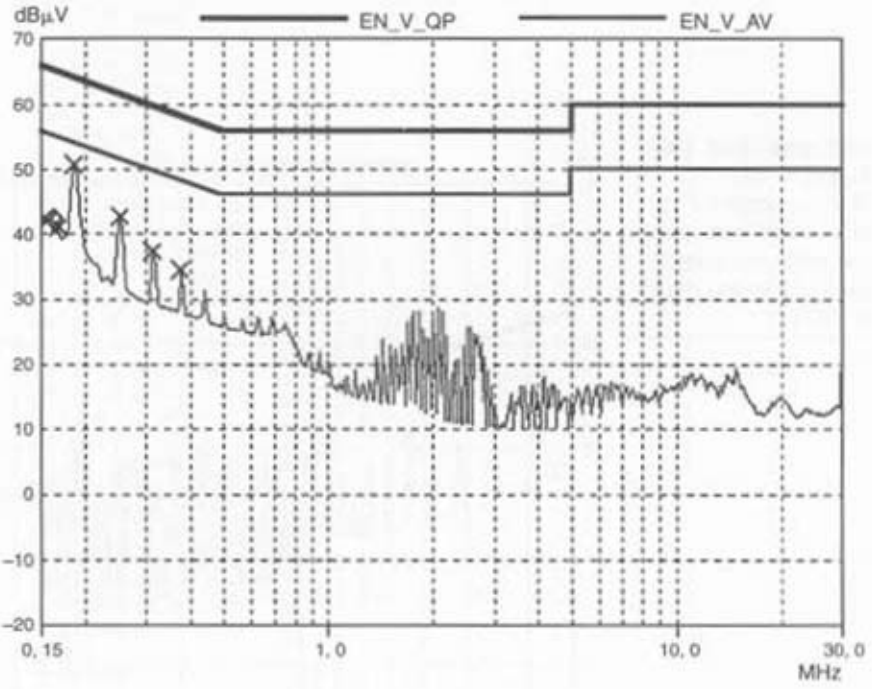


Figure C-4c
The final quasipeak DM-only measurement carried with an EMI receiver.

Total Noise Measurement

We now know that DM levels are within the limits. To attenuate the CM noise, we can wire a Y1-type capacitor between the primary and the isolated ground. For two-wire applications, the IEC950 standard limits the maximum leaking current to less than 250µA at 250VAC power supply. The maximum capacitor value you can use is thus: Zmin = 250V / 250µA = 1MΩ. With a 50Hz mains frequency, the Y capacitor cannot exceed: $\frac{1}{2 \cdot \pi \cdot 50 \cdot 1E6}$ = 3nF @ 50Hz or 2.6nF @ 60Hz. Start by wiring a 1nF Y1 capacitor or two 2.2nF Y2 in series if you want to reinforce the security in case one of the Y2 capacitor would fail shorted. Figure C-4d shows the final CM + DM plot in quasipeak and clearly testifies for the CISPR22 compliance. This measurement was also successfully carried in average at worse operating conditions (100VAC, 10W).

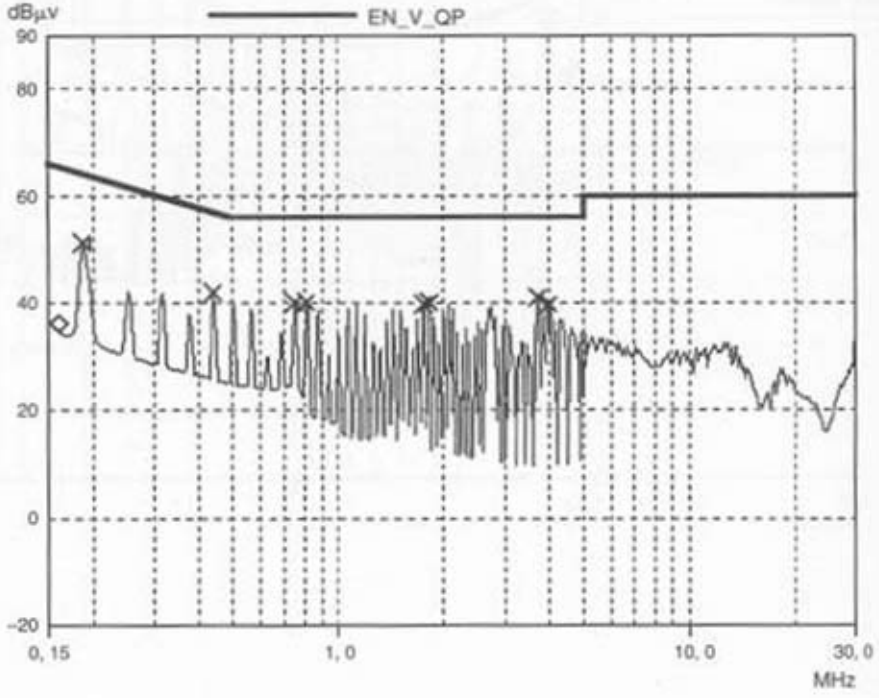


Figure C-4d
The composite QP plot carried over one line while the other is loaded (230VAC, Po = 10W).

If the test should fail in common mode, an option is to raise the CM inductor. Otherwise, you need to identify how noisy nodes can induce disturbances in adjacent copper traces or through the air. Carefully look at the rising time on the drain, how the output diode eventually rings, and various other unwanted ringings that could be snubbered by an RC network.

Line Impedance Stabilization Network SPICE netlist:

```
.SUBCKT LISN mainsN mainsL1 measN measL1 L1 N
*
L4 measL1 1 100nH
R9 1 0 1k
C7 1 2 1uF
L5 2 3 1.75mH
R10 3 0 100m
C8 2 L1 1uF
L6 L1 6 50uH
R11 6 7 10m
R12 7 8 3.33
C9 8 0 8uF
C10 7 0 10n
L7 7 10 250uH
R13 10 mainsL1 10m
C11 mainsL1 0 2uF
R3 mainsL1 0 100m
C4 measN 0 10pF
L2 measN 11 100nH
R5 11 0 1k
C5 11 12 1uF
L3 12 13 1.75mH
R6 13 0 100m
C12 12 N 1uF
L8 N 16 50uH
R7 16 17 10m
R8 17 18 3.33
C13 18 0 8uF
C14 17 0 10n
L9 17 20 250uH
R14 20 mainsN 10m
C15 mainsN 0 2uF
R17 mainsN 0 100m
.ENDS
*********
```

APPENDIX D

CD-ROM Content

The included CD-ROM contains the demonstration version of the following editors:

INTUSOFT ***ICAP/4*** (IsSpice) : www.intusoft.com

CADENCE ***PSpice*** : www.pspice.com

Spectrum-Software ***Micro-Cap*** : www.spectrum-soft.com

Powersim Technologies ***PSIM*** : www.powersimtech.com

Below are their respective revision numbers:

INTUSOFT Demo CD version 1.9

OrCAD Evaluation Software 9.1

MicroCap evaluation 6.1.3

PSIM demo version 4.1a

Each demonstration version is located in its eponymous subdirectory. Just go into the directory of your choice and follow the instructions. Please directly contact the software editors through their respective Web addresses if you encounter problems during the installation.

IsSpice4

Double-click on *Launch.exe* and see the program offering to install the demonstration version by default under c:\Spice8d. You can also choose to install the new version of IntuScope (Scope5), which offers enhanced capability compared to the previous implementation. Once this installation is done, drag and drop <IsSpice4\Chapter 5> directory from the CD to c:\Spice8d\Circuits\ or other equivalent path if you have selected another one. Book examples are located under this <Circuits> subdirectory. Please note that all examples are in read only, and you will need to modify their property to be able to save them when working. To do this, select all the files, right-click on the mouse, uncheck the read-only box, and you are set. You need to reboot the PC to further the installation.

OrCAD PSpice

On the CD, double-click on *OrCADStart.exe*. If you want to skip the demonstration video, just hit escape. Next, select install demo and check at least the following boxes to be able to run the examples: Capture CIS, PSpice A/D. To facilitate the examples extraction, please install the software in \Program Files\OrCAD. Once installed, quit the demo, go back to the CD, and double-click on <Book models\PSpice models.exe>, which will extract the files to \Program Files\OrCAD\PSpice\Averaged and Transient subfolders. From the adequat icon, run Capture and open either projects Average or Transient to simulate . . .

µCap

From the CD, launch *Setup.exe* and follow the instructions. There is nothing else to extract once finished; models are within the demo files. µCAP has placed the models in a subdirectory called <data> where A_xxxxx.cir and S_xxxxx.cir respectively denote Averaged and Switched examples.

PSIM

PSIM is extremely easy to install. Just double click on *psimdemo* located on the CD under <PSIM> subdirectory. Once done, drag and drop the rest of the files MC33260/261 (PFC examples) and the Flyback circuit under C:\PSIM if you have selected this path.

Some of the Chapter 3 examples will work on those demo versions, some will not, and the unlimited full version will be required to simulate them. If you are unfamiliar with a given software, the demo usually contains some tutorials in the form of movies (also known as INTUSOFT) or standard help files.

As you can imagine, writing and testing the models to finally translate them among the platforms has required a large amount of time. Despite the many efforts spent in testing the final versions, some bugs could still have escaped from the reviewer's attention. To correct these minor errors and make this book living once published, the author will maintain a Web page where new versions or model revisions will be posted. Its address is http://perso.wanadoo.fr/cbasso/.

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ABOUT THE AUTHOR

Christophe P. Basso is currently a technical engineer at ON Semiconductor (formerly Motorola Semiconductor) in Toulouse, France, where he derives the specifications of new offline controllers. He is a frequent contributor to *EDN Magazine's* "Design Ideas" section.